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THESIS

MODELING AND ANALYSIS OF A CONSTANT POWER SERIES-LOADED RESONANT CONVERTER

by

Richard B. Lebel

June 2011

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Future Naval systems and ships are being designed with pulse-power loads and hybrid electrical systems. There is a demand for efficient, reliable, and durable compact power converters to bridge pulse-power systems with the electrical plants of the future. This thesis presents modeling and analysis of a constant power Series Loaded Resonant (SLR) converter. The modeling work presented was successfully implemented in Simulink and then prototyped in a small-scale application in the laboratory. The Simulink model and prototype were tested under various conditions and may be used to reduce the risk in the design of future large-scale applications.

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MODELING AND ANALYSIS OF A CONSTANT POWER SERIES-LOADED RESONANT CONVERTER

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ABSTRACT

Future Naval systems and ships are being designed with pulse-power loads and hybrid electrical systems. There is a demand for efficient, reliable, and durable compact power converters to bridge pulse-power systems with the electrical plants of the future. This thesis presents modeling and analysis of a constant power Series Loaded Resonant (SLR) converter. The modeling work presented was successfully implemented in Simulink and then prototyped in a small-scale application in the laboratory. The Simulink model and prototype were tested under various conditions and may be used to reduce the risk in the design of future large-scale applications.

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LIST OF ACRONYMS AND ABBREVIATIONS

FPGA	Field Programmable Gate Array
IGBT	Insulated Gate Bipolar Transistor
ISE	Integrated Software Environment
PI	Proportional-Integral Controller
SDC	Student Design Center
SLR	Series-Loaded Resonant
ZCS	Zero-Current Switching

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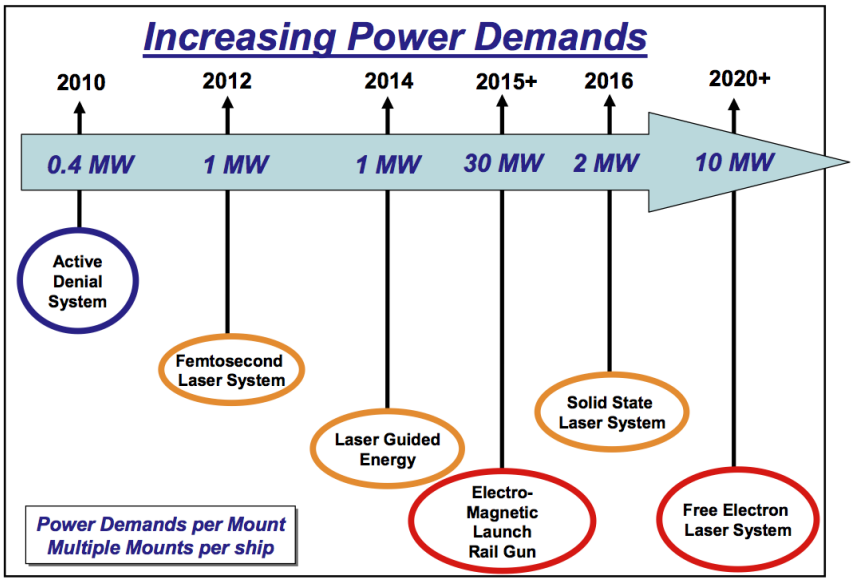
EXECUTIVE SUMMARY

The Navy's Next Generation Integrated Power System (NGIPS) is being designed to improve ship fuel economy and to provide energy for pulsed-power systems. Shipboard weapon systems in development are envisioned to have pulse-power requirements greater than 30MW, as illustrated below, which currently exceeds the power generation capability of today's fleet [1]. In line with NGIPS, the Navy also is researching energy storage options for pulsed-power loads that include capacitive, battery, and flywheel storage [2]. Energy stored in a battery may be moved to a capacitor bank through the use of a Series-Loaded Resonant (SLR) Converter.

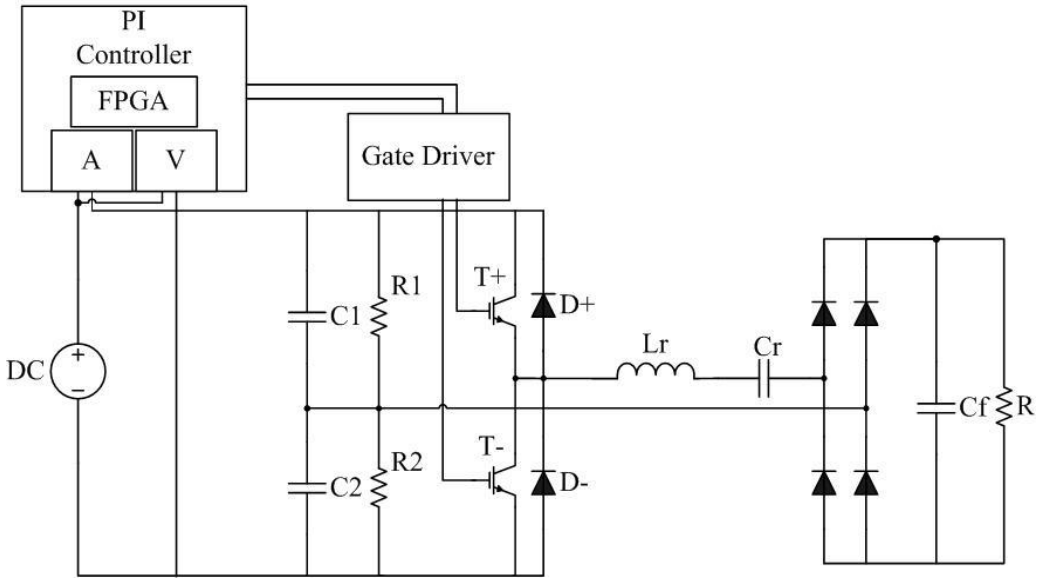


Shipboard power demands, from [1].

The objective of this thesis was to model a constant power SLR converter in Simulink and to validate the model in the laboratory with a hardware prototype. A validated physics-based model may then be scaled in and used to design a larger prototype with reduced risk.

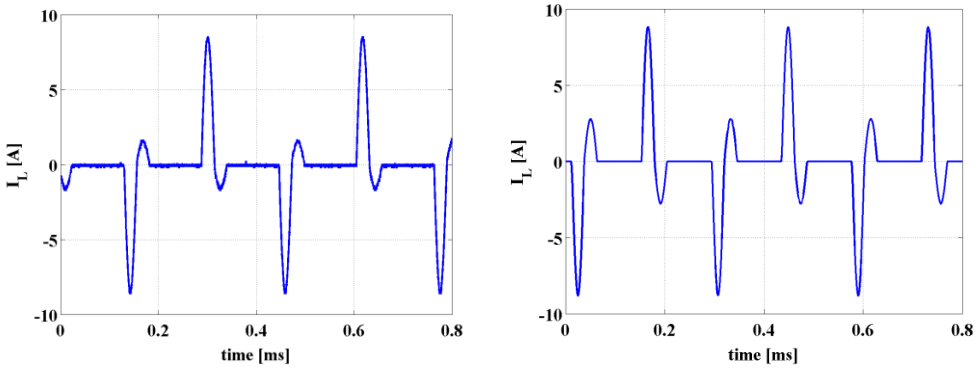
First, a constant power SLR converter Simulink model was developed. Then, using the Simulink model as a template, the Field Programmable Gate Array (FPGA) was programmed using a Xilinx Simulink System Generator toolbox. Using Naval

Postgraduate School's Student Design Center (SDC) [3] and a Semikron Semistack Multi-function Insulated Gate Bipolar Transistor (IGBT) box, we implemented the SLR converter illustrated below.



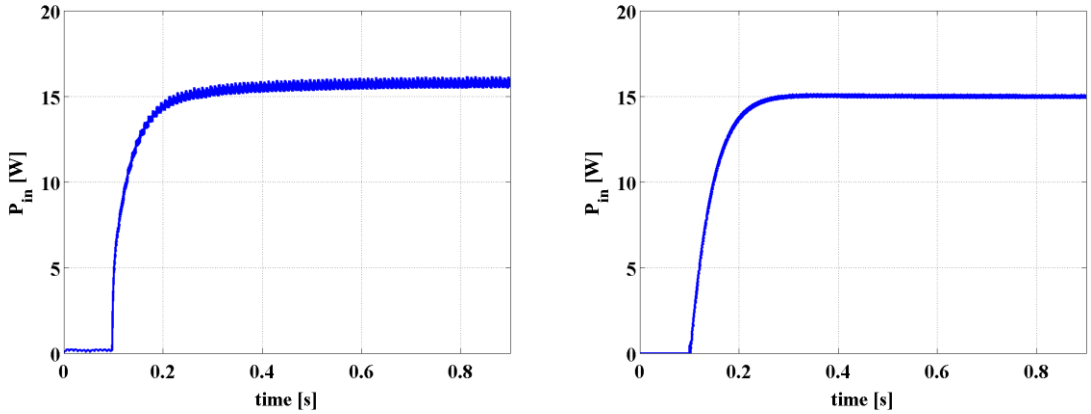
SLR Prototype.

A series of trials were run on the SLR prototype and compared to the simulation. The simulation and experimentally obtained resonant tank current is shown below, and it can be seen that the simulation closely predicts the behavior of the prototype. The slight variations in amplitude are attributed to conduction losses within the IGBTs and rectifier bridge.



Resonant tank current during steady state operation, experimental (left) and simulation (right).

The input power waveforms illustrated next show that the converter is tracking the commanded input power.



Input power during step response, experimental (left) and simulation (right).

In summary, a SLR converter was simulated in Simulink, and then the model was used as a template to program a FPGA. The model was then prototyped in the laboratory and used to validate the simulation where favorable results were achieved.

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I would like to thank my wonderful wife, Sarah, and my two wonderful children, Colin and Camille, for allowing me to engulf myself in my research. Your full support was always appreciated. I will always cherish the time we were able to spend as a family while stationed in Monterey.

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I would like to acknowledge Capt Joseph E. O'Connor (USMC), whom I have never met, for your outstanding research in 2008 that provided the Power Lab at NPS with a Student Design Center for employing FPGA based digital control of power electronics. The product of your work allowed me to perform research that would have otherwise been daunting. Thanks shipmate!

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I. INTRODUCTION

A. BACKGROUND

The Navy's Next Generation Integrated Power System (NGIPS) is being designed to improve ship fuel economy and to provide energy for pulsed-power systems. Shipboard weapon systems in development are envisioned to have pulse-power requirements greater than 30MW, as illustrated in Figure 1, which currently exceeds the power generation capability of today's fleet [1]. In line with NGIPS, the Navy is also researching energy storage options for pulsed-power loads that include capacitive, battery, and flywheel storage [2].

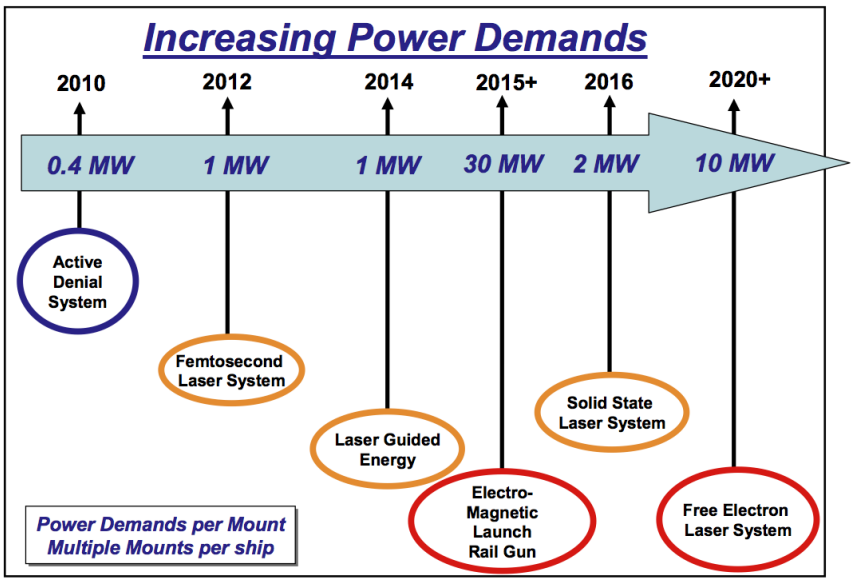

Figure 1. Shipboard power demands, from [1].

Energy may be stored in many ways; however, in order for it to be used, it has to be moved or transformed from one medium to another. As discussed in [3]–[7], Series-Loaded Resonant (SLR) converters are being researched to charge capacitors for use in pulse-power applications.

B. OBJECTIVE

It is possible to model virtually every aspect of a converter; however, a model only serves as a means to reduce time spent in the lab, production costs, and risk. A useful model predicts laboratory results and circuit dynamics, but can only be declared useful after experimental validation. The goal of this thesis is to develop a constant input power controller for a SLR converter in Simulink and to validate the model with a hardware prototype.

C. APPROACH

The first step was to select the circuit topology for the SLR converter. There are a multiple ways to design a SLR converter; however, the one implemented in this research was selected from [8] and is illustrated in Figure 2.

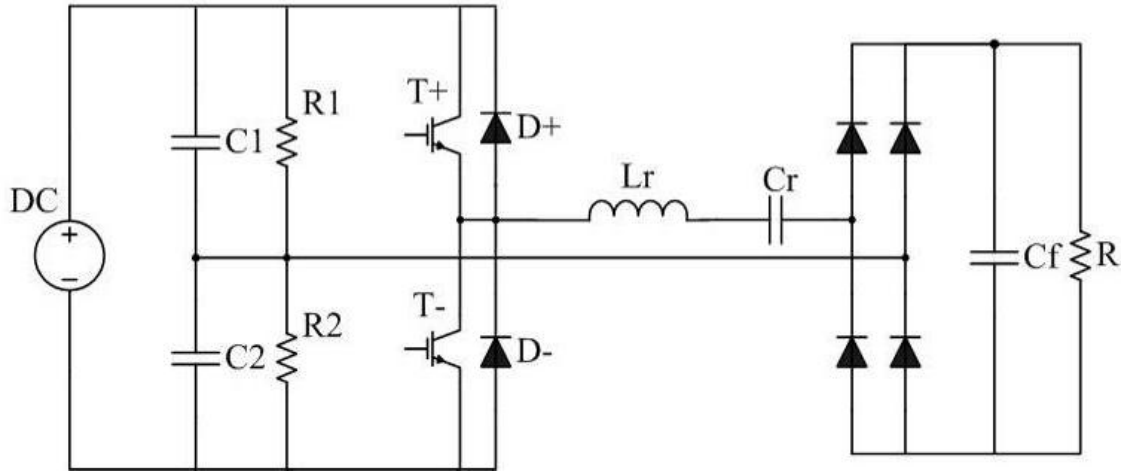

Figure 2. SLR converter.

With the circuit topology selected, the next step was to modify the existing SLR Simulink model [9] to provide the inputs and outputs required for a constant power control. The Simulink model was then configured with a proportional integral controller and was tuned to draw 15W of power while sourcing various loads. The model was then modified using the Xilinx Simulink toolbox and compiled to run a Xilinx XC4VLX25-10SF363 Field Programmable Gate Array (FPGA) embedded in

Naval Postgraduate School's Student Design Center [10]. The SDC was used to implement the control algorithm and trigger the gate drivers.

D. THESIS ORGANIZATION

SLR converter theory and operational characteristics are presented in Chapter II. The operational modes, advantages and disadvantages of the converter are explained in detail. A computer simulation model constructed in Simulink and the performance characteristics are included in Chapter III. A description of the Xilinx model, hardware prototype, equipment setup and performance is included in detail in Chapter IV. Results of the testing and conclusions about the Simulink model were compared to the measured results from the hardware prototyped SLR converter and are included in Chapter V. Recommendations for future research are included in Chapter VI.

Data sheets for the equipment used and the Matlab code are included in the Appendixes. Values for the equations developed in Chapter II-V are listed in Table 1 unless otherwise noted.

Table 1. Component values.

Parameter name	Value
Source voltage, VDC	43V
Resonant inductance, L_r	30 μH
Resonant capacitor, C_r	2.2 μF
Filter capacitor, C_f	4000 μF
Load, R	8.33 Ω
Distribution capacitors, $C_{1,2}$	2200 μF
Distribution resistors, $R_{1,2}$	22 $k\Omega$

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II. SERIES-LOADED RESONANT CONVERTER THEORY

A. INTRODUCTION

SLR converters are DC-DC converters with the output load connected in series with a resonant-tank as the name 'Series-Loaded Resonant' suggests. In this chapter, the theory of series-resonant circuits and converters is reviewed from [8]. The theory is applied to the system illustrated in Figure 2.

B. SERIES-RESONANT CIRCUIT THEORY

1. Overview

In order to understand how SLR converters operate, it is first necessary to analyze a series-resonant circuit. A series-resonant circuit is a commonly studied circuit in electrical engineering. The circuit consists of a series connected source, inductor, and capacitor and is illustrated in Figure 3.

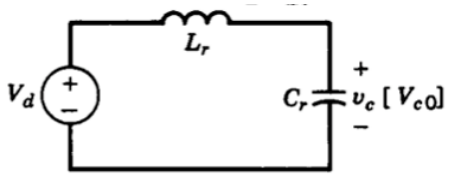

Figure 3. Undamped series-resonant circuit, from [8].

With the inductor current I_L and capacitor voltage v_c as state variables, (1) and (2) represent the circuit [8]:

$$L_r \frac{di_L}{dt} + v_c = V_d \tag{1}$$

$$C_r \frac{dv_c}{dt} = i_L \tag{2}$$

Solving (1) and (2) for v_c and i_L with $t > t_0$, we get [8]

$$i_L(t) = I_{L(0)}\cos\left[\omega_0(t-t_0)\right] + \frac{V_s + V_{c(0)}}{Z_0}\sin\left[\omega_0(t-t_0)\right] \tag{3}$$

$$v_c = V_s - \left(V_s - V_{c(0)}\right)\cos\left[\omega_0(t-t_0)\right] + Z_0 I_{L(0)}\sin\left[\omega_0(t-t_0)\right] \tag{4}$$

The waveforms from (3) and (4) are shown in Figure 4.

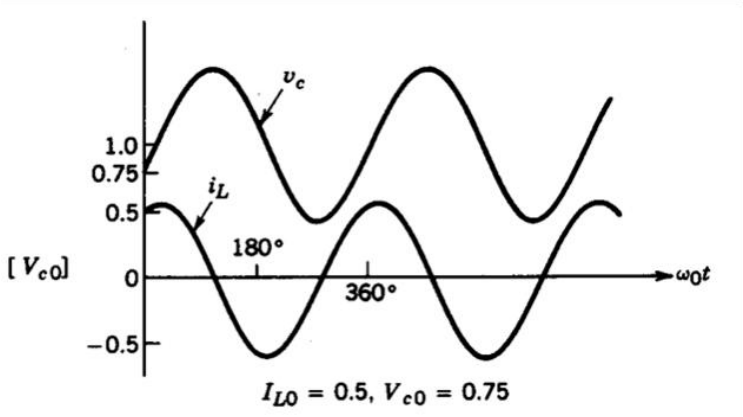

Figure 4. Undamped series-resonant circuit waveforms, from [8].

The resonance frequency ω_0 and characteristic impedance Z_0 of series-resonant circuits, evaluated with parameters from Table 1, are defined by

$$\omega_0 = 2\pi f_0 = \frac{1}{\sqrt{L_r C_r}} = \frac{1}{\sqrt{2.2\bullet10^{-6}\bullet30\bullet10^{-6}}} = \quad 1.2309\bullet10^5\,\frac{rad}{s} = 19.59kHz \tag{5}$$

$$Z_0 = \sqrt{\frac{L_r}{C_r}} = \quad 3.6927\Omega \tag{6}$$

2. Frequency Characteristics of a Series-Resonant Circuit

Adding a resistive load to a series-resonant circuit in Figure 3, we obtain the damped series-resonant circuit illustrated in Figure 5. The input impedance of the series-resonant circuit is expressed by

$$Z_{in} = X_{Lr} + X_{Cr} + R \tag{7}$$

When $X_{Lr} = -X_{Cr}$, then $Z_{in} = R$, which occurs when the circuit is operating at the resonant frequency of the circuit ω_0.

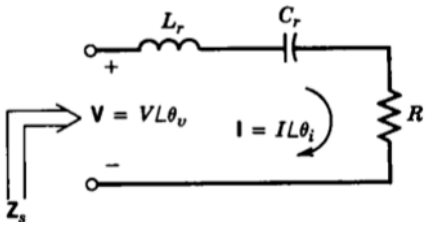

Figure 5. Dampened series-resonant circuit, from [8].

Sweeping the frequency of the input of the circuit in Figure 5 while measuring the input impedance, we get the results shown in Figure 6. At resonance, the impedance of the circuit is at minima and is equal to *R*. Above or below resonance, the circuit impedance increases. The relationship between the reactive and real parts of the circuit determines the quality factor Q_s. The slope of Q_s is an indication of how sensitive the circuit's impedance is to changes in frequency. SLR converters leverage the variable impedance characteristics of the series-resonant LC tank circuit in order to control the output current.

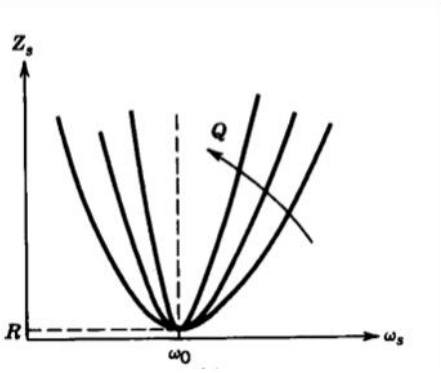

Figure 6. Frequency characteristics of a series-resonant circuit, from [8].

The quality factor of the circuit shown in Figure 5, evaluated with parameters from Table 1, is expressed by (8) [8]

$$Q_s = \frac{\omega_0 L_r}{R} = \frac{1}{\omega_0 C_r R} = \frac{Z_0}{R} = \frac{3.6927}{8.33} = 0.433 . \quad (8)$$

As can be seen from Figure 6, the switching frequency ω_s controls the impedance of the circuit Z_s and, the higher Q_s, the more sensitive Z_s will be to changes in ω_s.

C. SERIES LOADED-RESONANT CONVERTER THEORY

1. Converter Topology

The SLR converter prototyped in this research consisted a DC source, H-bridge, resonant-tank, output rectifier and filter/load are arranged as shown in Figure 7 and a controller, which is not shown. The converter is controlled by adjusting the driver pulses to IGBTs, $T+$ and $T-$, which will be discussed in detail in Chapter III.

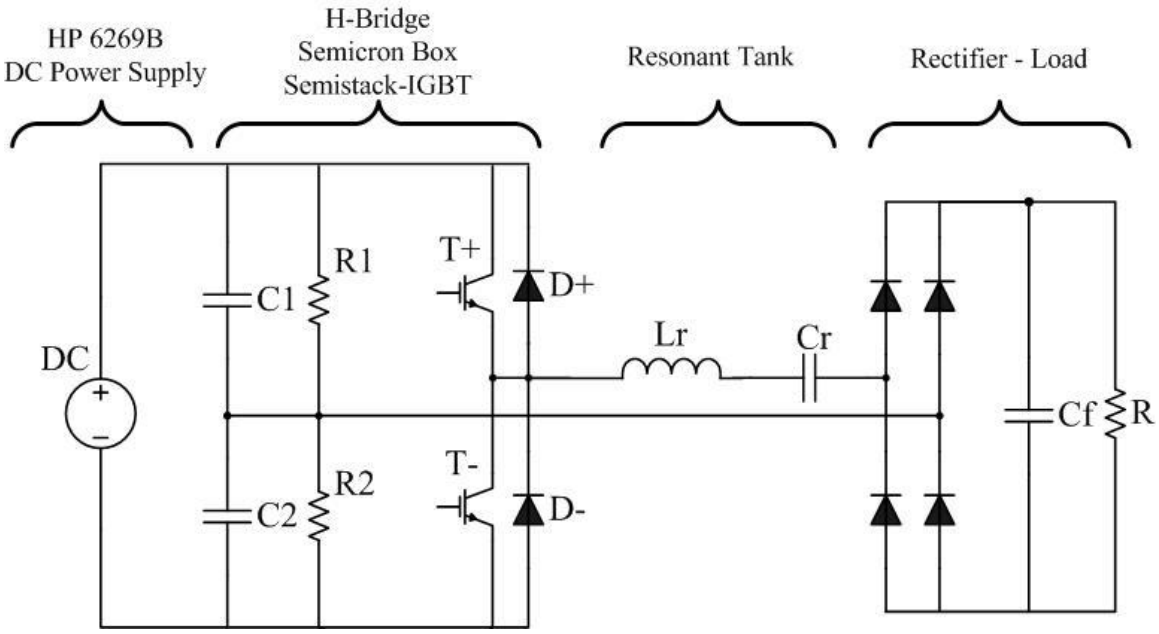

Figure 7. SLR converter diagram.

The mode of operation, operating frequency and peak voltage/current are factors that determine what type of switches are best suited for the SLR converter. The resonant tank subsection consists of an inductor L_r and capacitor C_r that form a series-resonant tank. A transformer may also be included in the resonant-tank subsection to provide

output voltage scaling and galvanic isolation between the input and output; however, the leakage inductance of the transformer must be added to L_r. This research did not include a transformer.

The rectifier subsection rectifies current pulses from the resonant tank and charges the output capacitor and sources the load. In order to simplify analysis, the capacitor at the output C_f is assumed to be large and capable of maintaining a constant output voltage across the load without relevant ripple.

2. Modes of Operation

SLR converters have three modes of operation: discontinuous-conduction mode (DCM) where $\omega_s < \omega_0 / 2$, continuous-conduction mode (CCM) where $\omega_0 / 2 < \omega_s < \omega_0$, and CCM where $\omega_0 < \omega_s$ [8]. In DCM, the inductor current goes to zero, whereas in CCM it does not. For simplicity, and other advantages that are discussed later, the converter was designed to remain in DCM. CCM modes are discussed in detail in [8].

The relationship between switching frequency ω_s and output current I_o is illustrated in Figure 8. While the converter is operating in DCM, the impedance of the resonant tank limits the output current, which is characteristic of a current source. A current source is desirable for shipboard applications because if the output or load were to fault, the converter would not fail. Additionally, once the fault is removed the converter can recover with no damage.

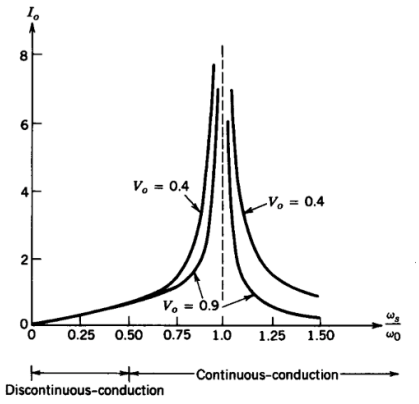

Figure 8. SLR converter normalized characteristics, from [8].

DCM operation may be described in six intervals as viewed from left to right in Figure 9. The intervals are described using the current waveforms. For a description of the voltage waveforms refer to [8].

When a voltage is applied to the series-resonant tank by gating $T+$ on, the tank resonates starting with a positive current pulse. When i_L is positive, current flows through $T+$(first interval). As i_L goes negative, current through $T+$ goes to zero and $D+$ turns on and remains on (second interval) until the energy stored in the tank is transferred to the load. At this point i_L remains at zero, awaiting the next switching event (third interval). When a voltage is applied to the series-resonant tank by gating $T-$ on, the tank is again excited and resonates starting with a negative pulse. With i_L negative, current flows through $T-$ if it is on (forth interval). As i_L goes positive, current through $T-$ goes to zero, and $D-$ turns on and remains on until the energy in the tank is transferred to the load (fifth interval). At this point i_L is zero, where it remains (sixth interval) until the cycle repeats. These six intervals are mapped into five states (the third and sixth intervals are identical) and are used to implement the converter in a Simulink state machine in Chapter III.

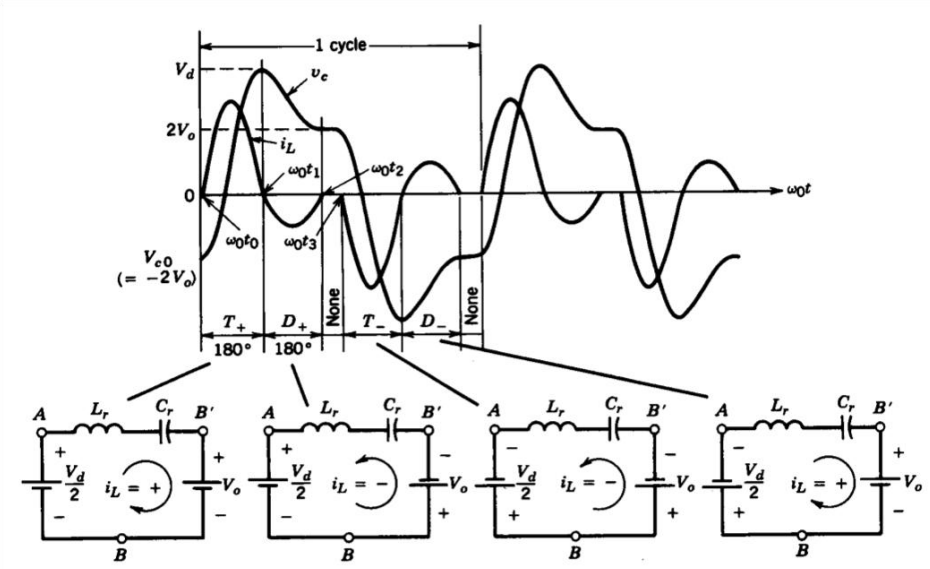

Figure 9. SLR converter: discontinuous-conduction mode, from [8].

3. Controllability

By adjusting the switching frequency ω_s, control of the output current of a SLR converter is achieved. SLR converters are commonly designed with closed loop control to regulate the output voltage [3]–[7]; however, in this research the control loop was closed to maintain constant input power to the controller.

The idealized input impedance of the SLR converter used in this research is illustrated in Figure 10. The red vertical line represents the boundary between DCM and CCM. By operating this converter between 1 kHz and 9.795 kHz, we see that the input impedance of the converter changes between $10 - 70\ \Omega$ as illustrated by the blue line. If the load is fixed at $8.33\ \Omega$, it can be concluded that the converter appears as a variable impedance between the source and the load.

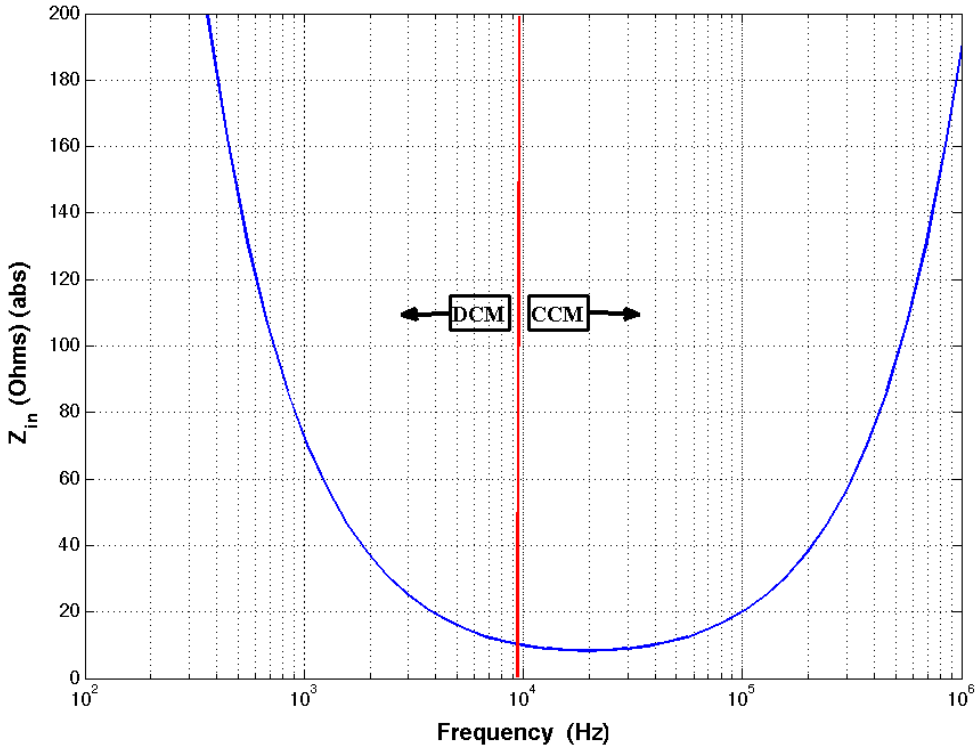

Figure 10. SLR converter input impedance vs. frequency plot (blue) and the boundary conditions between DCM and CCM (red).

4. Switching Losses

There are two types of losses associated with power devices and switching. The first type of loss is a result of the on-state resistance of the switch and is called a conduction loss. The second type of loss is the result of switching a device while it is conducting current or blocking voltage and is called a switching loss.

Conduction losses are a result of the on-state resistance of power devices and are generally much lower than switching losses. If voltage drop across an IGBT is defined as V_{ce}, and the current through the device is defined as I_o, then conduction losses are $p_{on} = I_o V_{ce}$ (in W). These losses are irrespective of switching frequency and may only be lowered by reducing I_o or by selecting a device with a lower V_{ce}.

Switching losses are the result of switching a device that is conducting current or blocking voltage. Because the device does not change states without a delay, there is an overlap between the current through the device and the voltage across the device that is realized as a loss $p_T = v_T i_T$, where the voltage across the device during switching defined as v_T and the current through the device as i_T form the switching loss p_T as illustrated in Figure 11.

Power converters may be either hard or soft switching converters. Hard switching refers to changing of states of a switch while it is conducting or blocking and is illustrated in Figure 11 and again in Figure 13 by the dotted line.

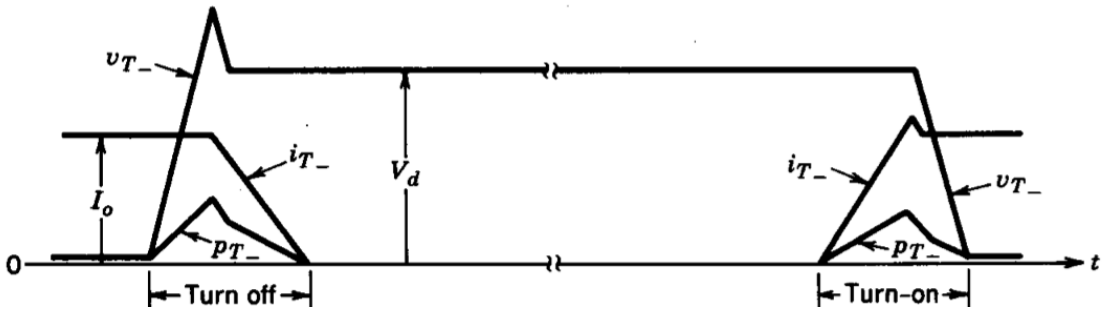

Figure 11. Hard switching voltage and current waveforms, from [8].

Soft switching converters are characterized by changing the state of the switch while the switch is not conducting or blocking voltage. If the switching loss is $p_T = i_T v_T$ and $i_T \approx 0$ or $v_T \approx 0$ during the switching event, then the loss is virtually eliminated.

The voltage and current waveforms in Figure 12 illustrate that the device is not conducting while the switch changes states, which is a form of soft switching called zero-current switching (ZCS). When the current in the circuit reverses, the antiparallel diode turns on and the device is then turned off, followed by the diode naturally commutating off. In this scenario, there are no switching losses realized.

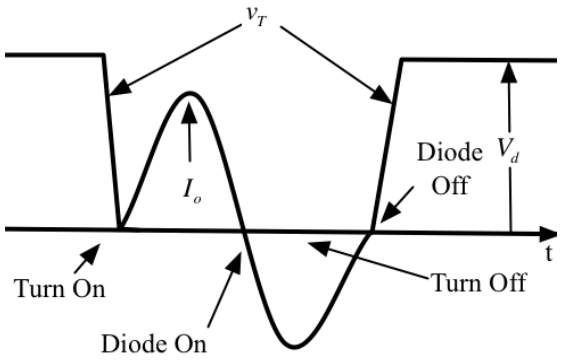

Figure 12. Soft switching voltage and current waveforms.

Soft switching is one of the advantages that SLR converters have over other converter topologies [8]. The solid line in Figure 13 illustrates soft switching, and the dashed line illustrates hard switching and the area under the curves are the switching losses (in W).

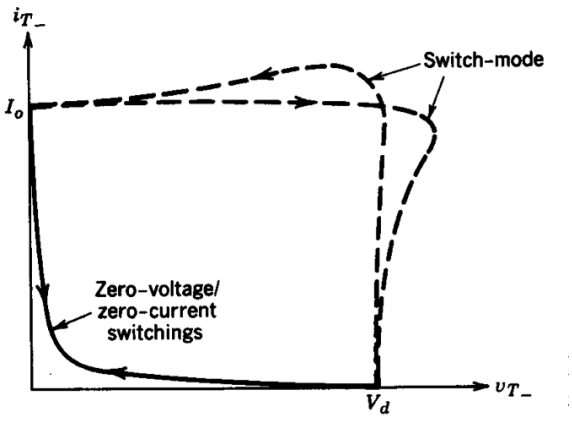

Figure 13. Hard vs. soft switching loci, from [8].

In hard switching, losses are directional proportional to the switching frequency, which limits the maximum switching frequency of the converter. Lower frequencies translate to larger converters that require more materials to build and subsequently weigh more. The stray inductive and capacitive components in the circuit coupled with hard switching introduces electromagnetic interference (EMI) problems [8]. Therefore, in addition to reduced switching losses, there are advantages to soft switching converters.

D. CHAPTER SUMMARY

In this chapter, an overview of series resonant circuits and their characteristics were presented. SLR converter topology characteristics, an in-depth analysis of the circuit operating in DCM, and switching losses were presented. In the next chapter, a detailed description of a Simulink model of a SLR converter is presented.

III. SLR SIMULINK/MATLAB MODEL

A. INTRODUCTION

In this chapter, a detailed description of the Simulink model used in this research is provided. The lossless model is composed of a Proportional-Integral (PI) controller, modulation, and converter blocks as arranged in Figure 14. The PI controller and modulation blocks were later used as source code in Chapter IV.

SLR converters may be designed to maintain constant voltage, current or power by adjusting the switching frequency of the converter. The converter in this research was modified from [9] to draw an average input power of 15 W while powering a load through the use of a PI controller. The PI controller adjusts the frequency of the converter to maintain the reference input power.

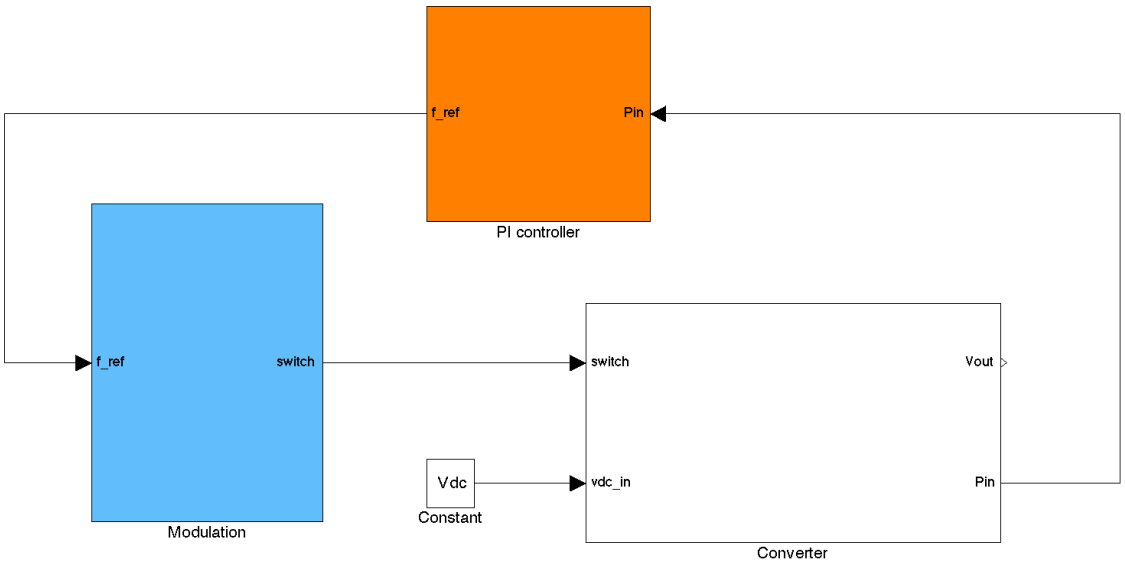

Figure 14. SLR converter Simulink block diagram.

B. PI CONTROLLER

The PI controller implemented in this research was configured with feed-forward input as illustrated in Figure 15. The feed-forward input was implemented to improve the response time and provide the converter with appropriate initial conditions.

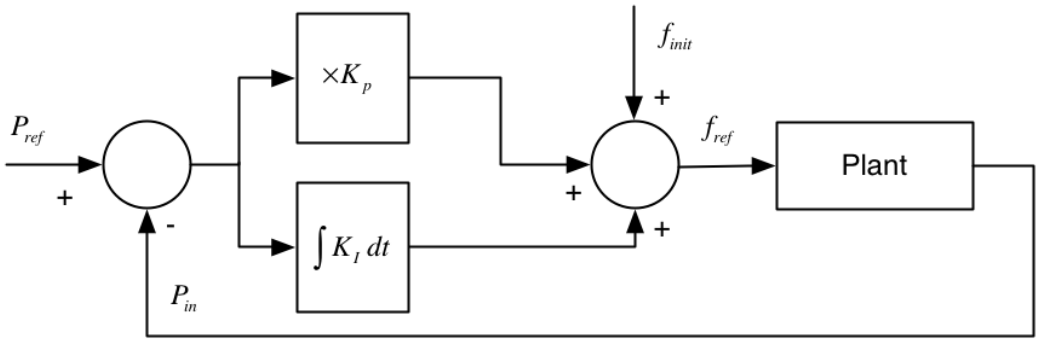

Figure 15. PI controller block diagram.

The PI controller subtracts the input power P_{in} from the reference power P_{ref} and generates an error signal, which represents the change in power required for the converter to reach steady state. The error signal is multiplied by K_p to generate the proportional error signal and is also multiplied by K_I and integrated to generate an integral error signal. The K_p and K_I error signals are summed and form an offset that is summed with the initial frequency f_{init} to produce

$$f_{ref} = f_{init} + \left(P_{ref} - P_{in}\right)\left(K_p + \int K_I dt\right). \tag{9}$$

The converter was adjusted to draw 15 W while sourcing an $8.33\,\Omega$ load with $K_I = 900$ and $K_p = 5$. Substituting K_I and K_p into (9), we get

$$f_{ref} = 3000 + \left(15 - P_{in}\right)\left(5 + \int 900 dt\right). \tag{10}$$

The PI controller implemented in the Simulink model is illustrated in Figure 16. The saturation block limits were set to $500 < f_{ref} < 8500$ in order to prevent the converter from transitioning into CCM.

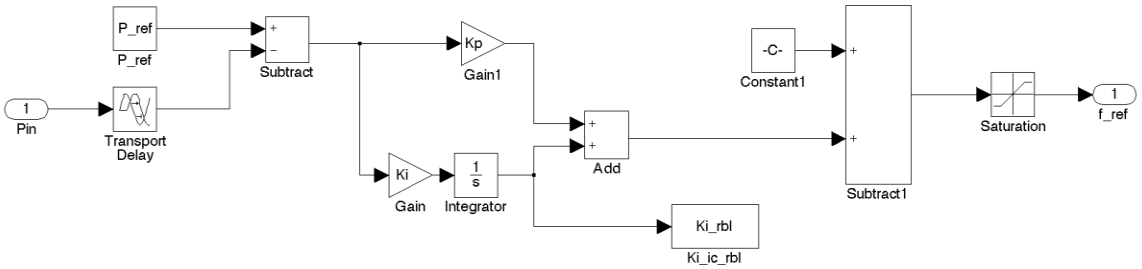

Figure 16. PI controller implemented in Simulink.

C. MODULATION

The modulation subsystem translates the output from the PI controller into gate pulses for the SLR converter as shown in Figure 14. In Figure 17 and Figure 18 f_{ref} is an input to the modulation subsystem that generates the trigger pulses ($T+$ and $T-$) for the IGBT gate drivers. The t_{on} and ramp signals are used to control the on time of the IGBT pulses and the switching frequency. The IGBTs must be on long enough to fully excite the LC network set by t_{on}, which is a function of the resonant frequency of the LC tank and given by

$$t_{on} = \frac{2pi}{\omega_0}\frac{1}{2}(1.1)(1.4) = \frac{4.8381}{\omega_0} \quad . \tag{11}$$

Equation (10) evaluated with $\omega_0 = 1.23 \times 10^5 rad/s$ yields $t_{on} = 39.3\mu s$.

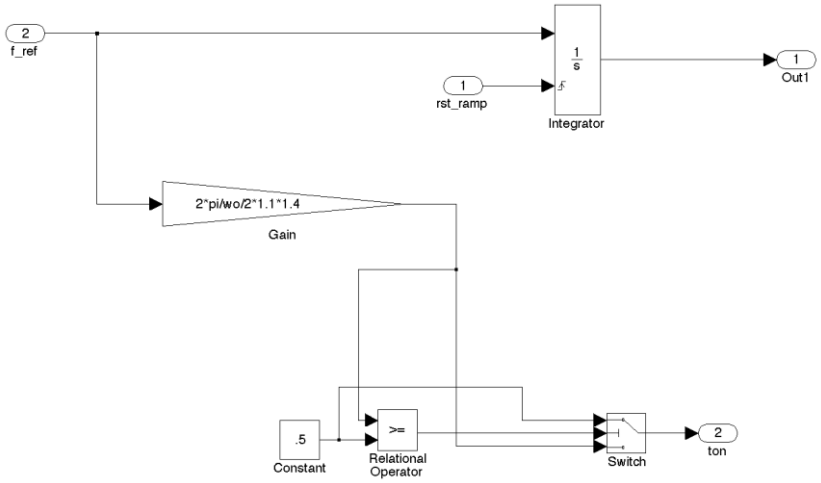

Figure 17. The ramp and t_{on} subsystem, after [9].

The output signal t_{on} controls the pulse widths of $T+$ or $T-$, which are created when the ramp passes the logical values set by the relation operators as illustrated in Figure 18.

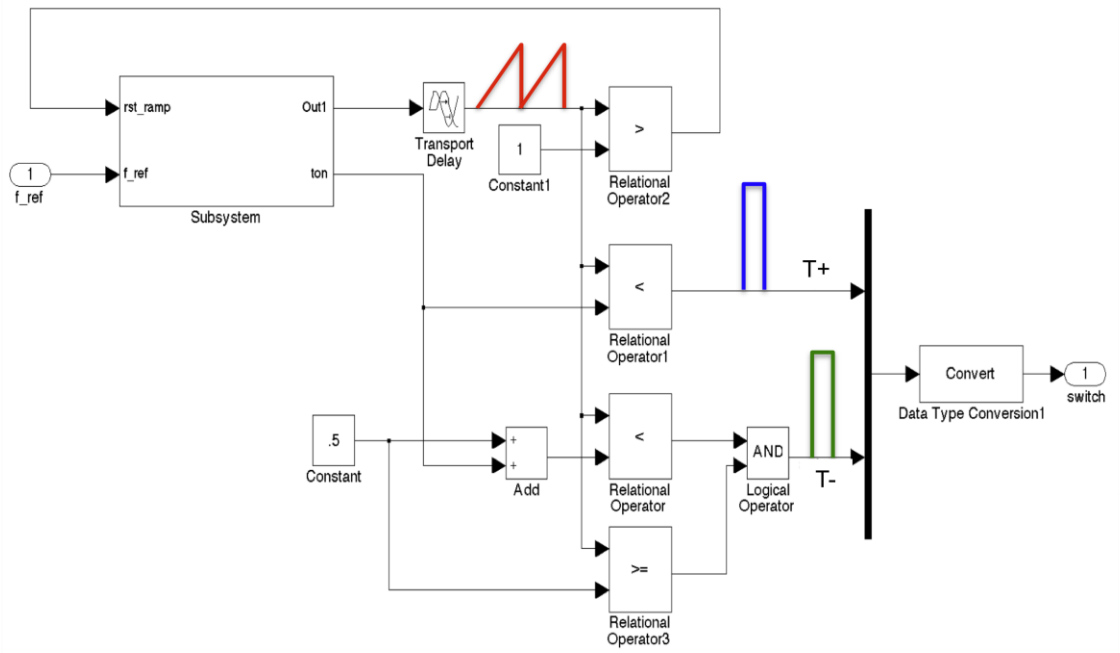

Figure 18. Modulation subsystem, after [9].

The ramp signal increases from 0 to 1 at the frequency commanded by f_{ref}. The $T+$ driver signal is set to 1 at $t=0$ and remains high until the time established by t_{on}. Once the ramp passes 0.5, $T-$ is set to 1 and remains on for the time established by t_{on}. The timing relationship between the ramp and t_{on} is illustrated in Figure 19.

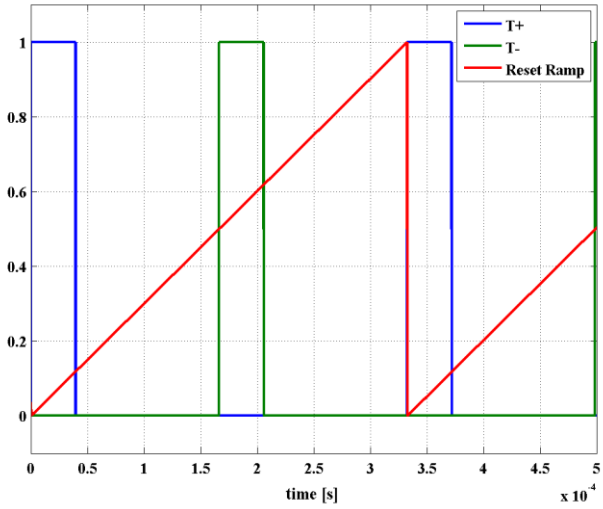

Figure 19. IGBT driver signals.

The resonant tank current and gate driver signals are related. In order for a SLR converter to ZCS, the gate driver signal must remain on long enough for the resonant current to reverse. Once the current reverses direction, the switch does not conduct current and may then be gated off. The switch must be gated off before the resonant current goes positive or the LC network will resonant a second time. The relationship between the gate pulse and the LC network used in this research is illustrated in Figure 20.

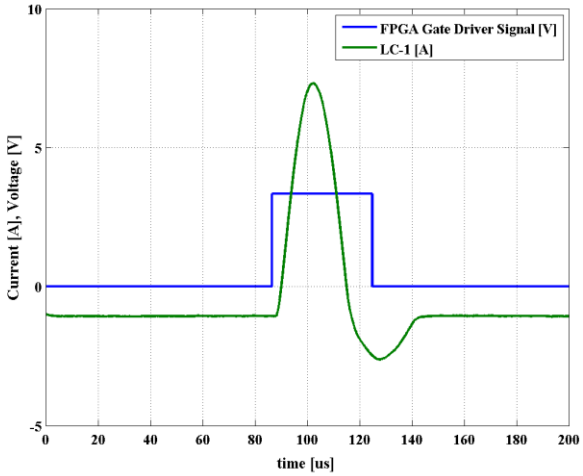

Figure 20. Gate driver signal and resonant tank current.

D. CONVERTER

The converter block is a physics-based model of the hardware used in this research. The converter is composed of two subsystems, the H-bridge and resonant tank and load, and is illustrated in Figure 21.

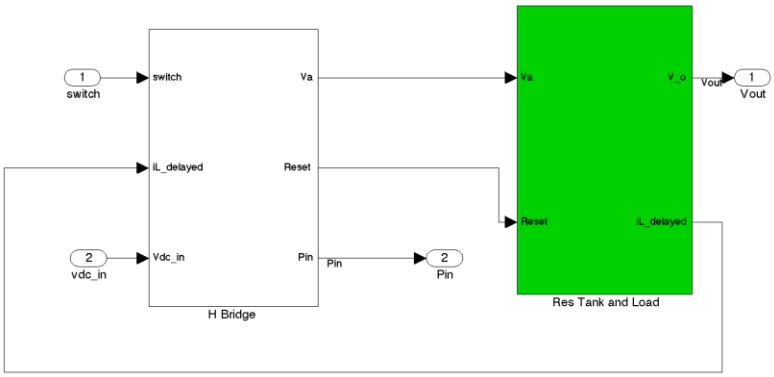

Figure 21. Converter subsystems.

The H-bridge was implemented through the use of a state machine [9] with the states listed in Table 2. The Simulink model of the state machine is illustrated in Figure 22. The states represent the different configurations that the switch and diodes transition through while the converter is operating in DCM. These states were previously described in Chapter II and illustrated in Figure 9. It can be seen in Table 3 that the H-bridge subsection mimics the behavior of a SLR converter in DCM operation. It is important to note that this portion of the model limits the converter to DCM. For CCM operation, this subsystem requires additional modeling effort.

Table 2. State description for the H-bridge subsystem.

S1	S2	S3	S4	S5
$T+=0$ $T-=0$ $D+=0$ $D-=0$	$T+=1$ $T-=0$ $D+=0$ $D-=0$	$T+=0$ $T-=1$ $D+=0$ $D-=0$	$T+=0$ $T-=0$ $D+=0$ $D-=1$	$T+=0$ $T-=0$ $D+=1$ $D-=0$

Table 3. State transition matrix for the H-bridge subsystem.

Current	Next				
	S1	S2	S3	S4	S5
S1		$T+$	$T-$		
S2				$\overline{T+} / I_L > 0$	$I_L < 0$
S3				$I_L > 0$	$\overline{T-} / I_L < 0$
S4	$\overline{T-} / I_L < 0$	$T+$			
S5	$\overline{T+} / I_L > 0$		$T-$		

Based on the mapping of the state transition matrix shown in Table 3, the state machine passes $T+$, $D+$ and the resonant tank current to the inverter. The inverter operates in a symmetric manner; therefore, $T-$ and $D-$ are not required in the inverter subsection and were terminated as illustrated in Figure 22.

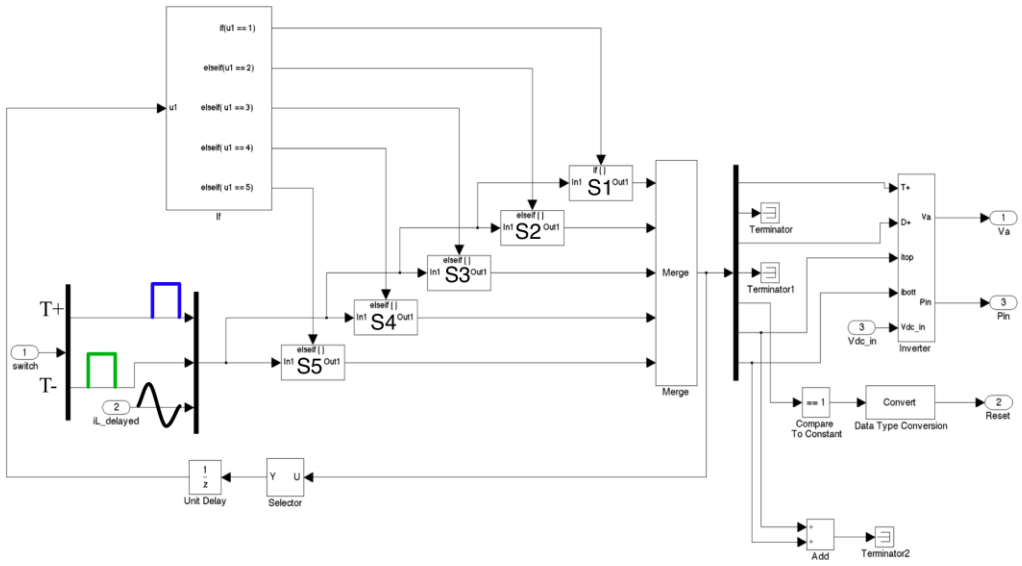

Figure 22. H Bridge subsystem, after [9].

The inverter subsystem takes inputs $T+$, $D+$, and input current and voltage and generates the input power P_{in} and V_a as illustrated in Figure 23. The i_{top} and i_{bott} inputs are the current that is being removed from the capacitor by the converter each time the IGBTs are gated on. Resistors R_1 and R_2 represent the leakage resistance in capacitors C_1 and C_2. The leakage current that is flowing through R_1 and R_2 is accounted for by subtracting it from the input current. The output V_a routes voltage from either the C_1 or C_2 to the resonant tank and load based on $T+$ and $D+$. The parameters L_1 and R_{L1} represent the source inductance and losses.

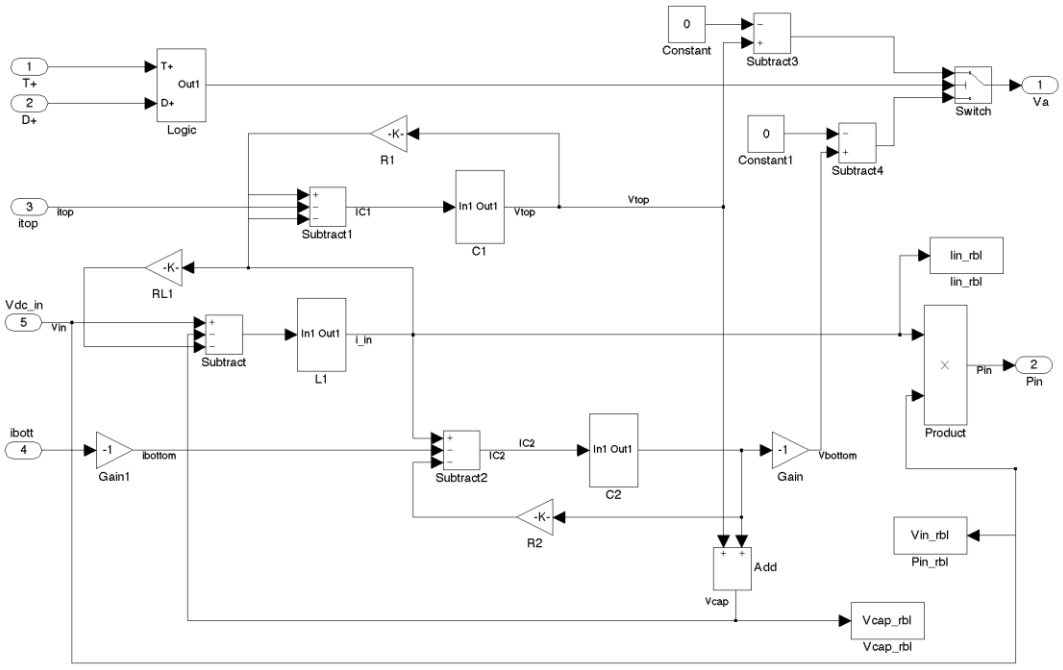

Figure 23. Inverter, after [9].

The inverter modeled in this research does not account for temperature effects or switching losses and may be a topic for future work.

The resonant tank and load are illustrated in Figure 24. The output of the inverter V_a sources the tank circuit and load. The reset input to the integrator used to implement

the resonant tank current ensures that the tank current returns to zero as during each cycle. Various signals are mapped to variables and were used to generate the plots included in Chapter IV.

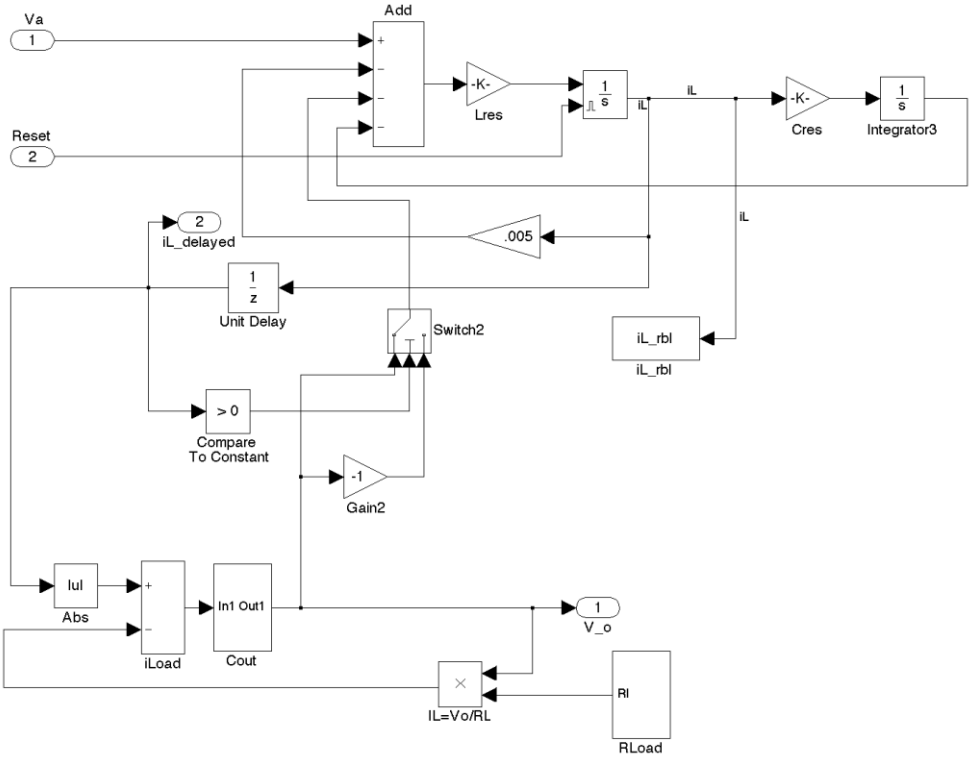

Figure 24. Resonant tank and load, after [9].

E. CHAPTER SUMMARY

In this chapter, a detailed description of the Simulink model used in this research was provided. The lossless model is composed of a PI controller, modulation, and converter blocks as arranged in Figure 14. The modeling was done in a manner that allows for the PI controller and modulation subsections to be used as the template for the Xilinx code that was used to program a FPGA in the SLR prototype in the next chapter.

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IV. SLR PROTOTYPE

A. INTRODUCTION

In this chapter, the hardware implementation of the SLR prototype is discussed in detail. The circuit topology and controller scheme theory were discussed in detail in Chapters I and II. The prototype consists of the hardware illustrated in Figure 7 and the PI Controller and Modulation subsystems illustrated in Figure 14. The prototype consists of two parts, the FPGA controller and converter hardware.

B. FPGA CONTROLLER

The first step in prototyping the SLR converter was replacing the Simulink blocks with Xilinx blocks using the Xilinx System Generator Toolbox. The advantage of modeling first with Simulink and then with the Xilinx System Generator Toolbox is that the Simulink model is easier to debug and also provides a tool to make modifications to the controller for future work.

The Xilinx FPGA controller was based on the model used in [9], which utilized the SDC developed in [10]. The SDC consists of a Virtex-II reference board, Xilinx XC4VLX25-10SF363 FPGA, and four port Voltage and Current Analog-to-Digital converters [10]. The SDC is interfaced to a personal computer (PC) via a Joint Test Action Group (JTAG) cable. The SDC measures the input power and implements PI control expressed by Equation (9) and then outputs the gate driver signals. The one aspect of the Xilinx System Generator Toolbox that is different than the Simulink blocks is that Xilinx blocks are going to be translated to code that will be written to a FPGA that has a finite real estate and computing power, which require the processor to use Fixed-Point numbers.

1. Fixed-Point Numbers

Hardware components interpret numbers as defined by their data type. In this research, signed and unsigned fixed-point numbers were used. The position of the binary point is the means by which fixed-point values are scaled and interpreted.

A binary representation of a generalized fixed-point number is shown in Figure 25 where: bi is the ith binary digit, wl is the word length in bits, b_{wl-1} is the location of the most significant bit (MSB), and b_0 is the location of the least significant bit (LSB) [11].

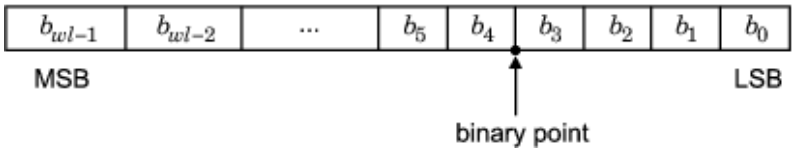

Figure 25. Fixed-Point Number, from [11].

Signed, fixed-point numbers are characterized by the word length in bits *a*, the position of the binary point *b*, and the sign. The set of numbers realizable is finite and is defined as α. Signed data uses two's complement to represent numbers and has a range that is expressed by [12]

$$A(a,b) = -2^{a-1} \le \alpha \le 2^{a-1} - 2^{-b} \quad (12)$$

In a Xilinx Simulink block, a signed fixed-point number with 13 bits that has two bits to the right of the decimal point is represented by Fix_13_2. Substituting $a = 13$ and $b = 2$ into (12), we get a range of -4096 to 4095.75.

Unsigned, fixed-point numbers are characterized by the word length in bits *a* and the position of the binary point *b*. The set of numbers realizable is finite and is defined as α. The range of an unsigned fixed-point number is expressed by [12]

$$A(a,b) = 0 \le \alpha \le 2^{a} - 2^{-b} \quad (13)$$

In a Xilinx Simulink block, an unsigned fixed-point number with 13 bits that has two bits to the right of the decimal point is represented by Ufix_13_2. Substituting $a = 13$ and $b = 2$ into (13), we get a range of 0 to 8191.75.

2. Xilinx FPGA Controller

The controller implemented in this research is illustrated in Figure 26. The controller consists of a PI controller, modulation, and shutdown timer blocks and are

illustrated in Figure 27 through Figure 29. The data conversion and Chipscope interface blocks were included for debugging purposes. The controller also passes four channels of data from the FPGA to the Chipscope interface after being formatted in the Data conversion subsystem.

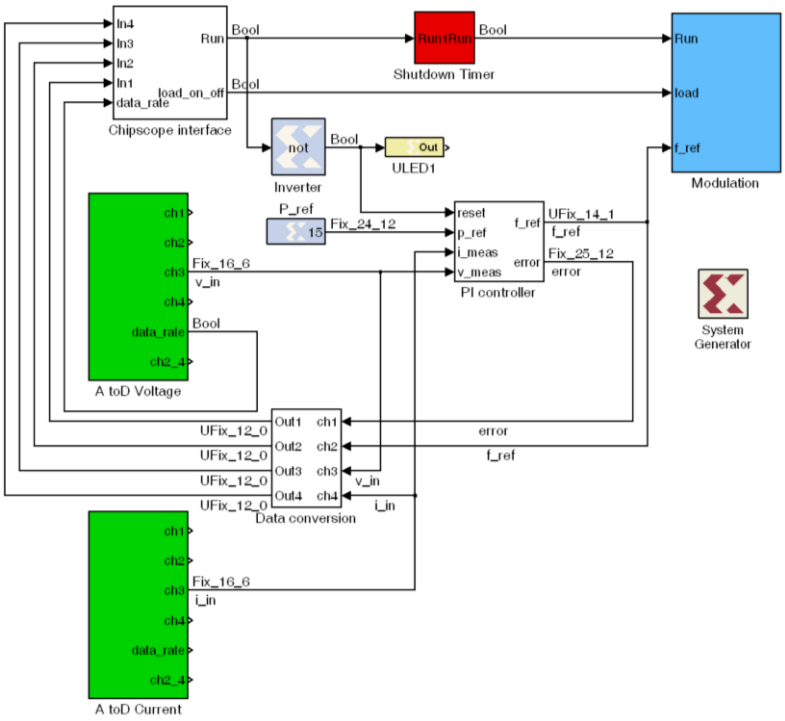

Figure 26. Xilinx Simulink model, after [9].

a. PI Controller

The PI controller implemented in the Xilinx model is a discrete version of the model discussed in detail in Chapter II and is illustrated in Figure 27. The output of this model was limited by the word size of the AddSub1 (UFix_14_1), which when substituted into (11), yields 8191.5 Hz.

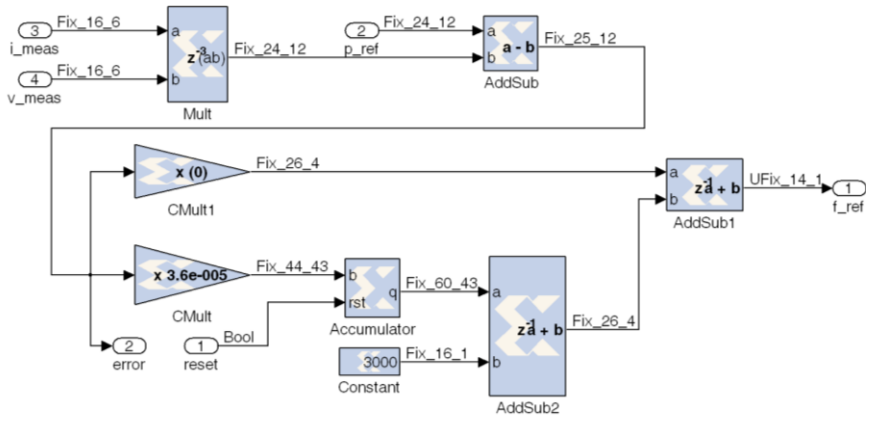

Figure 27. PI controller subsystem.

b. Modulation Subsystem

The Modulation subsystem implemented in the Xilinx model is identical in theory to the model discussed in detail in Chapter II and illustrated as Figure 28. The modulation subsystem accepts the f_{ref} generates the gate driver pulses for the hardware. The blocks on the right side of Figure 28 are the outputs of the system and are mapped to pins on the FPGA.

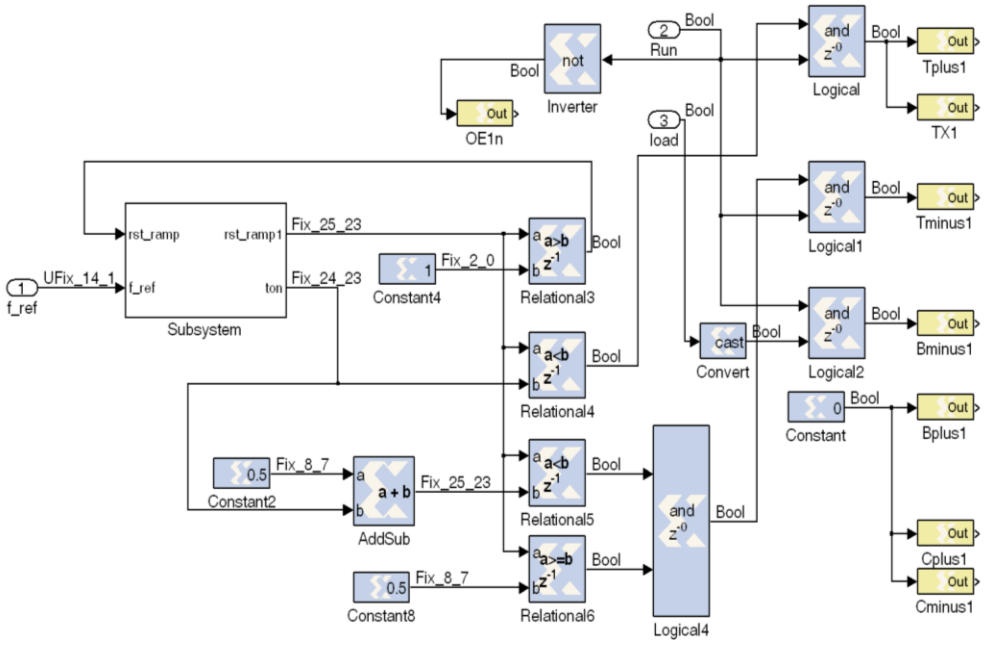

Figure 28. Modulation subsystem, after [9].

c. Shutdown Timer

The shutdown timer implemented in the Xilinx model is illustrated in Figure 29. The timer consists of a SR flip-flop with a counter that latches the output low once the counter reaches a predetermined value. The output latch requires RUN1 to be high in order for the output to go high. This feature removes the timing glitches associated with the initialization of Inverter1.

The shutdown timer was designed with a SR Flip Flop that latches off once the clock count exceeds a constant. In constant power operation the converter in this research was powered off by a timer after two seconds of operation:

$$t_{stop} = \frac{cycles}{clock(Hz)} = \frac{50 \times 10^6}{25 \times 10^6} = 2 \text{ s} \qquad (14)$$

.

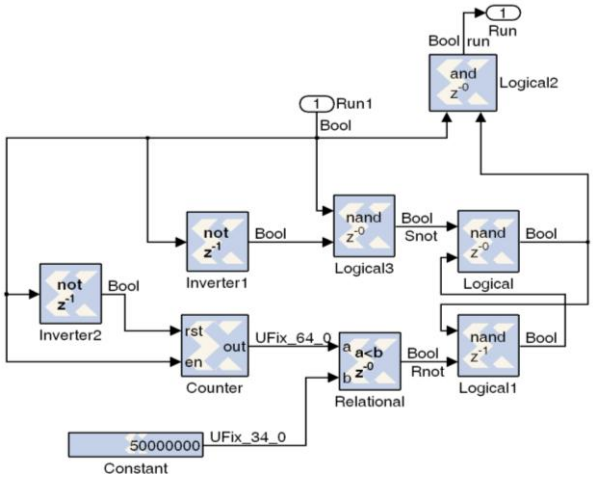

Figure 29. Shutdown timer.

3. FPGA Programming

The Simulink model was modified using three software packages to format the model to program the FPGA as illustrated in Figure 30.

Figure 30. Software flow diagram.

First, Simulink reads the Matlab initial condition file, included in Appendix B, which contains the variables required for the application. Second, the Xilinx System Generator toolbox generates HDL code and outputs a ".ise" file. Third, the output of the Xilinx System Generator is converted to a ".bit" file using Xilinx ISE Design Suite. Finally, the ".bit" file is then downloaded to the FPGA via a JTAG cable using Chipscope. Once the FPGA is programmed, it is interfaced through a GUI within Chipscope and may be debugged and analyzed in real time using the Chipscope to Matlab interface included in Appendix B.

C. HARDWARE

The hardware used to implanted the converter was a package by SEMIKRON called SEMISTACK-IGBT. The package consists of a three-phase inverter that is coupled to a capacitor bank. The inverters inside the SEMISTACK are made of SKM 50 GB 123D IGBTs that are controlled by a SEMIKRON SKHI 22 gate drivers.

The SLR converter was described in Chapter I and illustrated in Figure 7. In this research, the Semicron Box containing SKM 50 GM 123 IGBTs with SKHI 22 gate drivers was utilized, and the datasheet is included in Appendix A. The values for the other components are listed in Table 1.

D. CHAPTER SUMMARY

With the FPGA programmed, the prototype was configured as illustrated in Figure 31. A series of tests were performed on the Simulink model from Chapter II and was used to establish the parameters required for the converter to maintain constant power. The results of these trials are presented in Chapter IV.

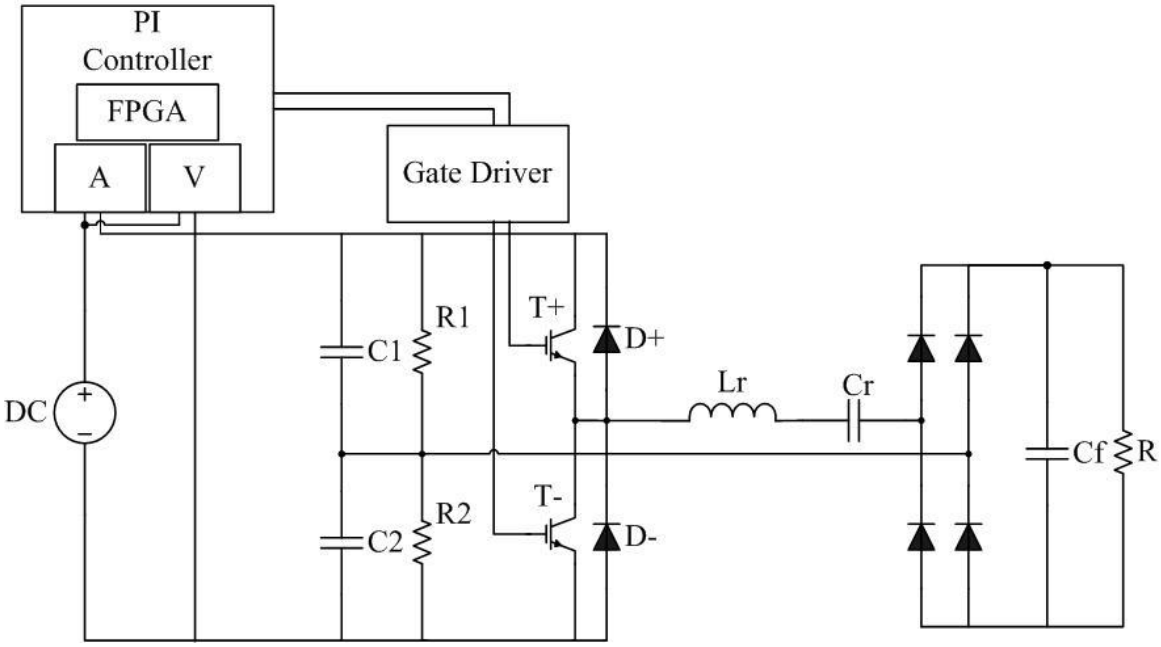

Figure 31. SLR prototype model.

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V. RESULTS

A. OVERVIEW

In this thesis, a constant power SLR converter was simulated in Simulink by closing the control loop on the input power. The Simulink model was then used to develop the code to program the Xilinx FPGA using the Xilinx System Generator toolbox in Simulink. A series of tests were performed on the Simulink model and compared to the hardware prototype, which was configured as illustrated in 0

In order for a model to be useful, the results from the simulation must reasonably predict the behavior of the physical system. It is important to note that acceptable results leave room for interpretation in defining whether the model is useful or not. The results of the trials performed in this research are presented in this chapter.

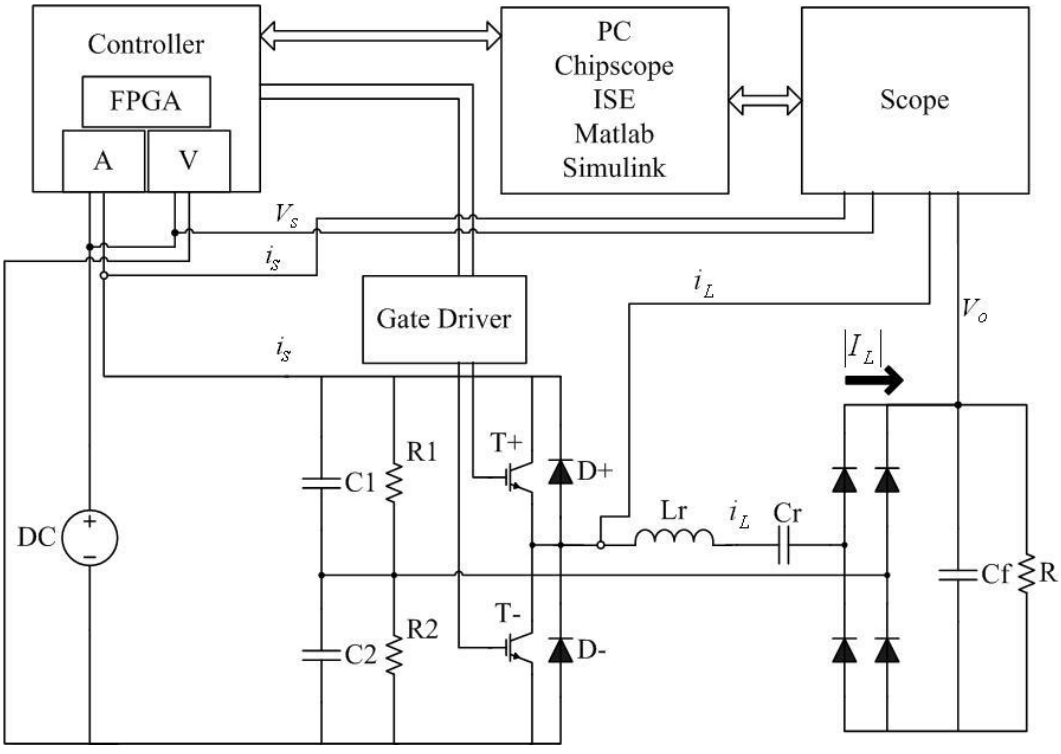

Figure 32. SLR converter test setup.

B. EXPERIMENTS

Three trials were run on the hardware, and the waveforms included in this chapter were downloaded from the oscilloscope filtered through a low pass filter and formatted in Matlab and included as "experimental" plots. The Matlab code to format the oscilloscope data for Matlab is included in Appendix B. Identical trials were run on the software model by running Simulink from the terminal with a Matlab script, which is included in Appendix B. The results filtered through a low pass filter

$$H(j\omega) = \frac{3000}{3000 + j\omega}. \tag{15}$$

The filtered data was formatted in Matlab and are included as "simulation" plots. A description of the experiments is included as Table 4.

Table 4. Experiment description.

Trial	$V_{in}(V)$	R (Ω)
1	42.90	8.33
2	37.00	8.33
3	42.90	12.28

C. EXPERIMENT RESULTS

The simulation reasonably predicted the hardware performance with the exception of the output voltage and power levels. The disparity between these measurements were a result of not accounting for the IGBT and full wave rectifier losses and present an area for further modeling work.

Additionally, the shape of the input power and output power waveforms reveal that the simulation does not capture all aspects of the source and load. The disparity

between the shapes of these waveforms could be an area for future research. The other areas where the model does not accurately predict the performance of the hardware are detailed in the results.

1. Trial 1

In Trial 1, the input voltage to the converter was set to 42.9 V and the load was fixed at $8.33\,\Omega$. The step response and steady state performance of the converter was measured and simulated. The output voltage, input power, output power, and resonant tank current waveforms were compared and illustrated in Figure 33 through Figure 37. The results of the trial are summarized in Table 5.

The converter was tuned to operate with this input voltage and load. All of the parameters measured correlated with the expected values with the exception of the output voltage, output power and switching frequency.

Table 5. Trial 1 results.

Parameter	Experimental	Simulation
Output Voltage Rise time [ms]	123	104
Input Power Rise time [ms]	111	99
Output Voltage [V]	8.71	11.14
Input Power Response	Critically Damped	Critically Damped
Mean Input Power[W]	15.23	15.00
Mean Output Power[W]	9.38	14.92
Peak Resonant Tank Current [A]	8.65	8.85
Switching Frequency [kHz]	3.14	3.55

The output voltage of the converter was measured after the converter was turned on through the Chipscope interface, and the results are illustrated in Figure 33. An oscilloscope recorded the converters output voltage and is displayed on the left. A comparable experiment was conducted on the Simulink model, and the results are displayed on the right.

The appreciable disparity between the two results is the steady state value of the output voltage. The experimental results reached steady state at 8.71 V, while the simulation reached steady state at 11.14 V. The differences between the plots are a result of the Simulink model's lossless characteristics. While the converter is conducting, there are two diode voltage drops in the full bridge rectifier V_d in series with the on-state IGBT voltage drop V_{ce} that are not accounted for in the model. Assuming that these voltage drops are the source of the disparity, we have $V_{loss} = 2V_d + V_{ce}$. If $V_d \approx 0.7$ V and $V_{ce}\big|_{8A} \approx 1.0$ V, then $V_{loss} \approx 2.4$ V. Given that the difference between the recorded results are due to losses, then $V_{out(\exp)} = V_{out(sim)} - V_{loss(sim)}$ and $V_{out(\exp)} \approx 11.15 - 2.4 \approx 8.75$ V. Therefore, it can be concluded that the disparity between the simulation is largely a result of not accounting for the voltage drops of the devices in the simulation. If these parameters were included in the model, then more favorable results would likely be achieved.

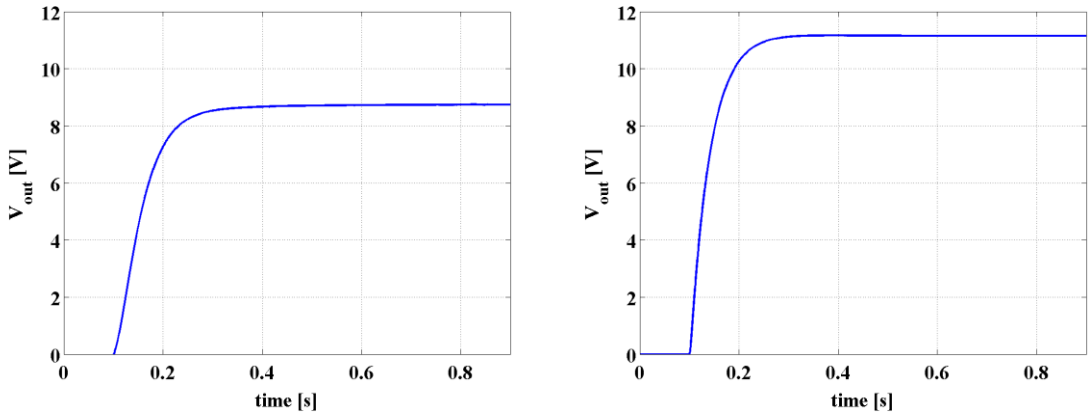

Figure 33. Trial 1 output voltage step response, experimental (left) simulation (right).

The input power of the converter was measured after the converter was turned on through the Chipscope interface, and the results are illustrated in Figure 34. An oscilloscope recorded the converter's input current and input voltage and then calculated the input power. The input power was downloaded to a PC, filtered in Matlab, and is displayed on the left. A comparable experiment was conducted on the Simulink model, and the filtered results are displayed on the right.

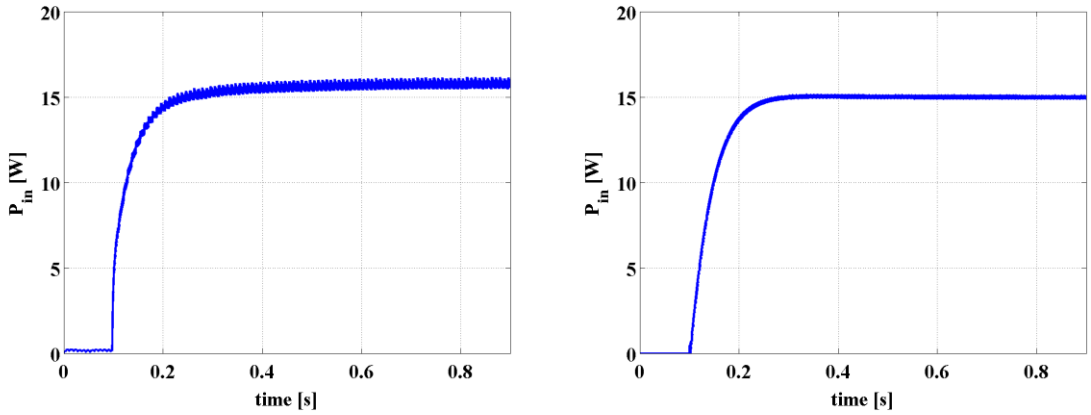

Figure 34. Trial 1 input power step response, experimental (left) simulation (right).

The experimental input power was slightly higher than the simulation until the converter fully reached steady state as observed in Figure 35. The steady state input power waveforms have a similar mean value shown in green; however, the simulation did not capture the same input power waveform as the experiential data. The difference in the shape of these waveforms is attributed to voltage source characteristics that were not modeled in this research.

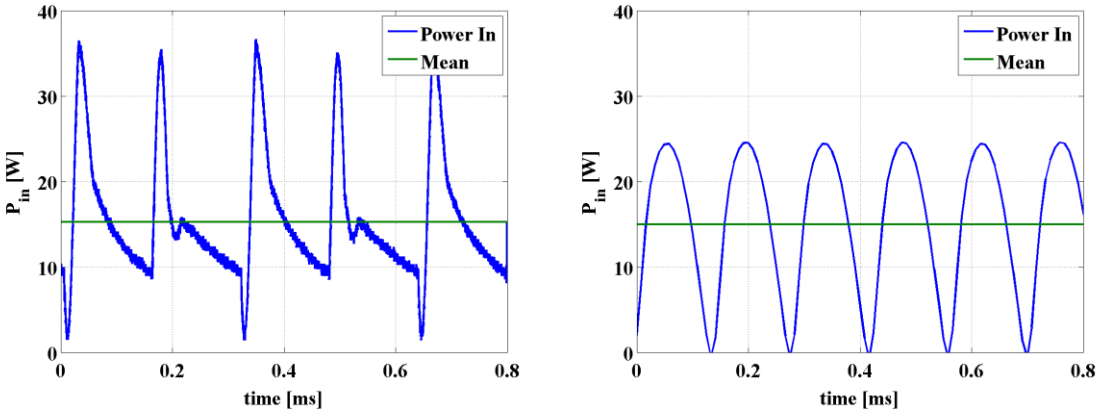

Figure 35. Trial 1 input power during steady state operation, experimental (left) and simulation (right).

The steady state output power is illustrated in Figure 36. The left plot is experimental data, and the right is from the Simulink simulation. The simulation's mean output power was 14.92 W and the experimental output power was measured at 9.38 W. The difference between the two values is 5.54 W and is attributed to the losses realized by the IGBT and full bridge rectifier.

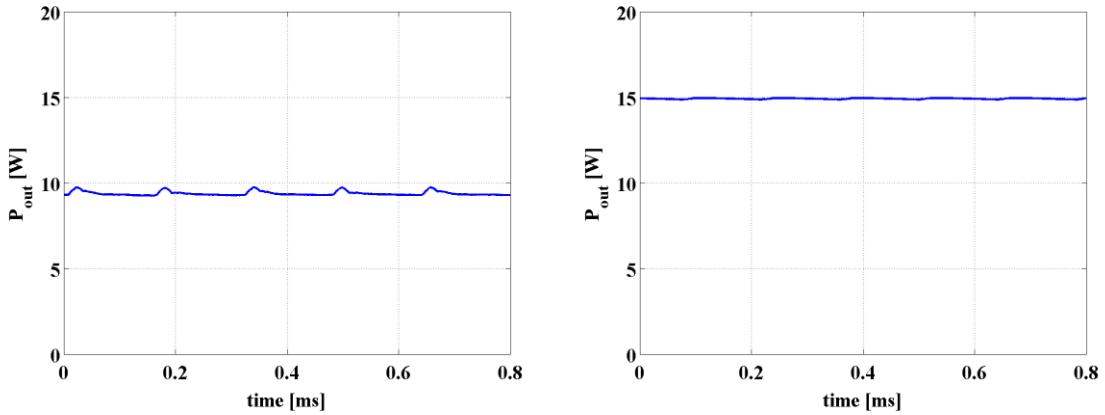

Figure 36. Trial 1 output power during steady state operation, experimental (left) and simulation (right).

The steady state resonant tank current is illustrated in Figure 37. The experimental data is displayed on the left, and the simulation on the right. The experimental model operated at 3.14 kHz, while the simulation operated at 3.55 kHz. In steady state the experimental model's peak current was measured at 8.65 A and the smaller peak was measured at 1.55 A. The simulation's peak current was measured at 8.85 A, and the smaller peak was measured at 2.78 A. The disparity between the smaller peaks is a result of the differences in output voltages between the experimental data and the simulation.

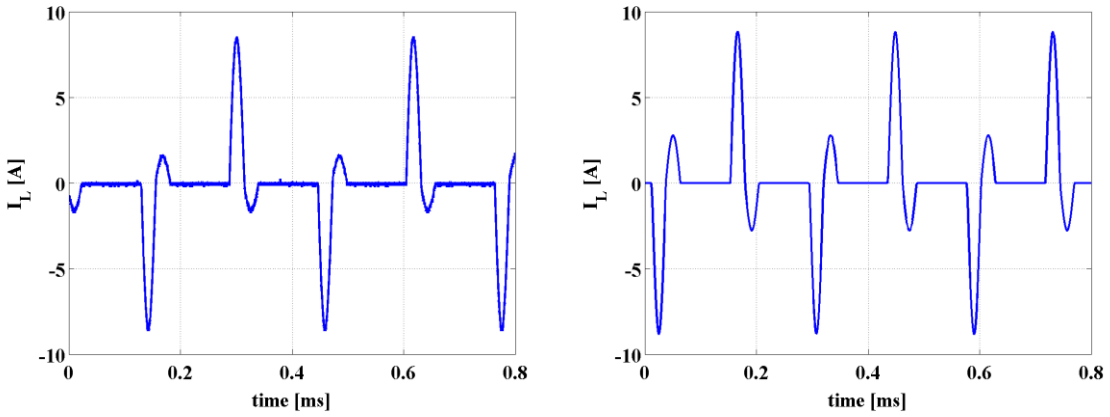

Figure 37. Trial 1 resonant tank current during steady state operation, experimental (left) and simulation (right).

2. Trial 2

In Trial 2, the input voltage to the converter was set to 37 V and the load was fixed at $8.33\,\Omega$. The step response and steady state performance of the converter was measured and simulated. The output voltage, input power, output power, and resonant tank current waveforms were compared and illustrated in Figure 38 through Figure 42, and the results are summarized in Table 6.

Table 6. Trial 2 results.

Parameter	Experimental	Simulation
Output Voltage Rise time [ms]	74	152
Input Power Rise time [ms]	74	204
Output Voltage [V]	9.15	11.14
Input Power Response	Critically damped	Critically damped
Mean Input Power [W]	16.03	15.00
Mean Output Power [W]	10.05	14.93
Peak Resonant Tank Current [A]	7.75	8.03
Switching Frequency[kHz]	3.55	3.75

The output voltage of the converter was measured after the converter was turned on through the Chipscope interface, and the results are illustrated in Figure 38. An oscilloscope recorded the converter's output voltage, which is displayed on the left. A comparable experiment was conducted on the Simulink model, and the results are displayed on the right.

The appreciable disparity between the two results is the steady state value of the output voltage. The experimental results reached steady state at 9.15 V, while the simulation reached steady state at 11.14 V. The differences between the plots are likely a result of the Simulink models lossless characteristics as discussed in detail in Trial 1's analysis.

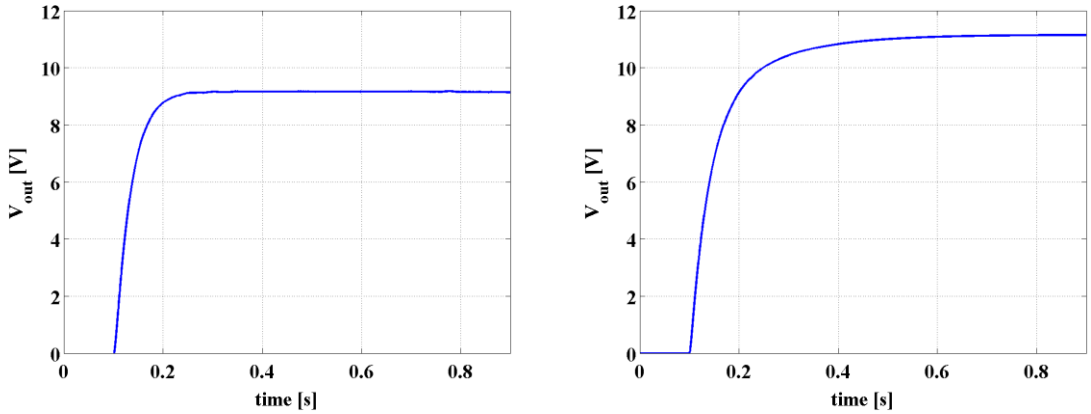

Figure 38. Trial 2 output voltage step response, experimental (left) simulation (right).

The input power of the converter was measured after the converter was turned on through the Chipscope interface, and the results are illustrated in Figure 39. An oscilloscope recorded the converter's input current and input voltage and then calculated the input power. The input power was downloaded to a PC, filtered in Matlab, and displayed on the left. A comparable experiment was conducted on the Simulink model, and the filtered results are displayed on the right. A critically damped response was observed in both the hardware and simulation.

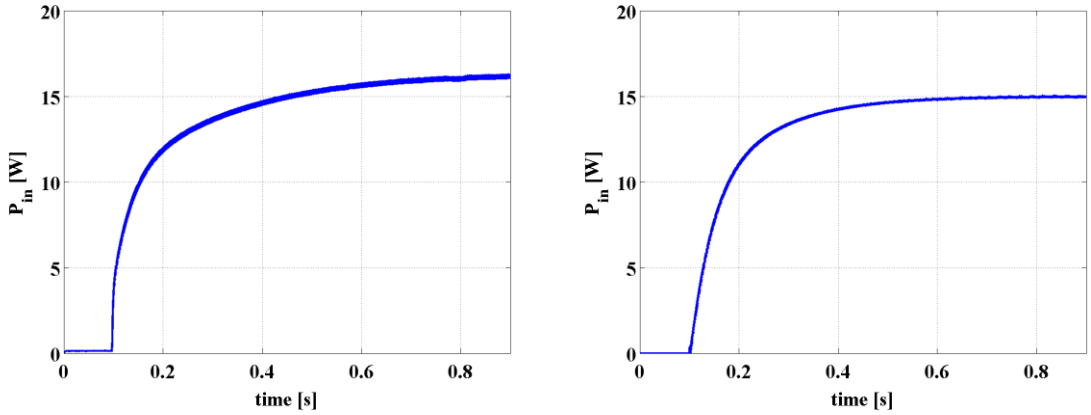

Figure 39. Trial 2 input power step response, experimental (left) simulation (right).

The steady state input power waveforms are illustrated in Figure 40. The hardware model reached steady state at 16.02 W where the simulation achieved steady state at the commanded 15 W. During testing, the PI controller performed as designed and drove the error signal to zero; therefore, the 1.02 W difference is the result of measurement error and presents an opportunity for further research. Furthermore, if the converter were to be operated at a higher power level, the 1.02 W difference may be determined irrelevant.

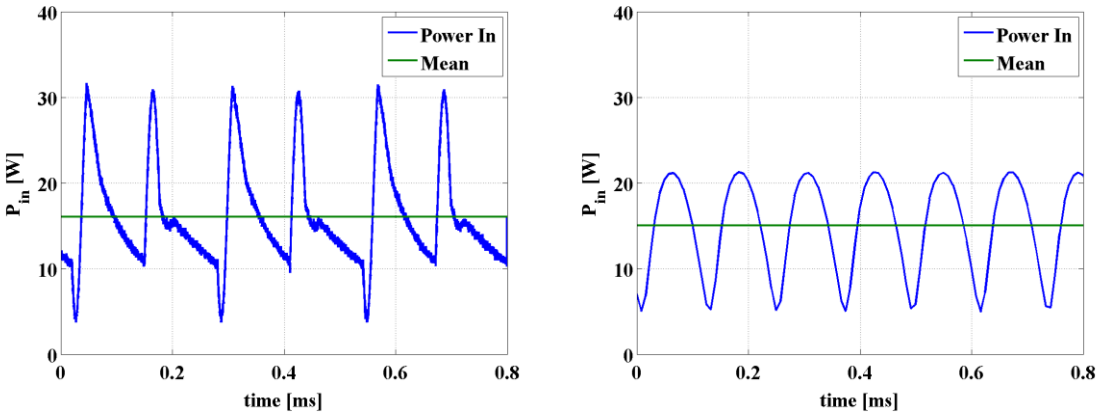

Figure 40. Trial 2 input power during steady state operation, experimental (left) and simulation (right).

The steady state output power is illustrated in Figure 41. The left plot is experimental data, and the right is from the Simulink simulation. The simulation's mean output power was 14.93 W, and the experimental power out was measured at 10.05 W. The difference between the two values is 4.88 W and is attributed to the losses realized by the IGBT and full bridge rectifier.

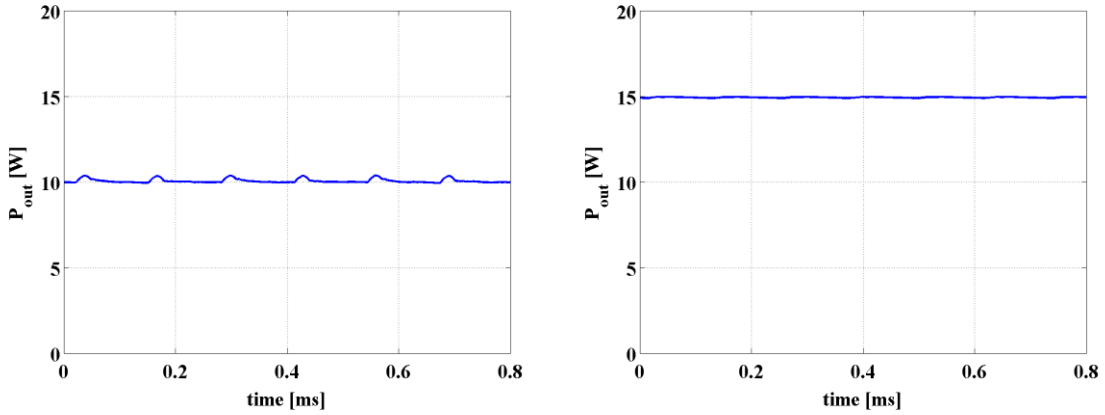

Figure 41. Trial 2 output power during steady state operation, experimental (left) and simulation (right).

The steady state resonant tank current is illustrated in Figure 42. The experimental data is displayed on the left, and the simulation on the right. The experimental model operated at 3.55 kHz, while the simulation operated at 3.75 kHz. In steady state the experimental model's peak current was measured at 7.75 A, and the smaller peak was measured at 0.96 A. The simulation's peak current was measured at 8.05 A, and the smaller peak was measured at 1.95 A. The disparity between the smaller peaks is a result of the differences in output voltages between the experimental data and the simulation.

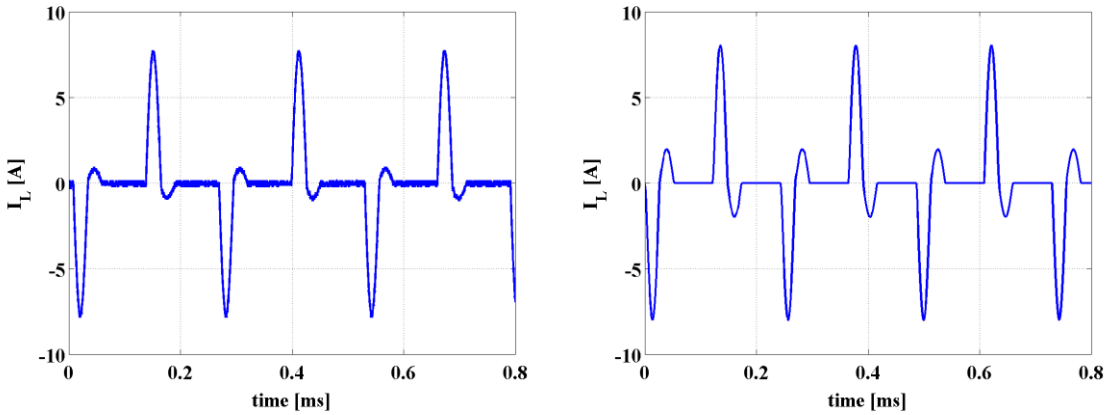

Figure 42. Trial 2 resonant tank current during steady state operation, experimental (left) and simulation (right).

3. Trial 3

In Trial 3 the input voltage to the converter was set to 42.9 V and the load was increased to 12.28 Ω. The step response and steady state performance of the converter was measured and simulated. The output voltage, input power, output power, and resonant tank current waveforms were compared and illustrated in Figure 43 through Figure 46, and the results are summarized in Table 7.

Table 7. Trial 3 results.

Parameter	Experimental	Simulation
Output Voltage Rise time [ms]	117	224
Input Power Rise time [ms]	113	294
Output Voltage [V]	12.09	14.6
Input Power Response	Underdamped	Underdamped
Mean Input Power [W]	15.35	15.01
Mean Output Power [W]	10.2	14.92
Peak Resonant Tank Current [A]	9.2	9.75
Switching Frequency [kHz]	2.54	2.70

The output voltage of the converter was measured after the converter was turned on through the Chipscope interface, and the results are illustrated in Figure 43. An oscilloscope recorded the converter's output voltage, which is displayed on the left. A comparable experiment was conducted on the Simulink model, and the results are displayed on the right.

The appreciable disparity between the two results is overshoot associated with the step response. The experimental results reached steady state at 12.12 V, while the simulation reached steady state at 14.6 V. The differences between the plots are a result of the Simulink models lossless characteristics as discussed in detail in Trial 1's analysis.

The experimental results reached steady state after a peak input voltage of 12.94 V (6.7% overshoot). The simulation reached steady state after a peak input voltage of 16.31 V (11.7% overshoot).

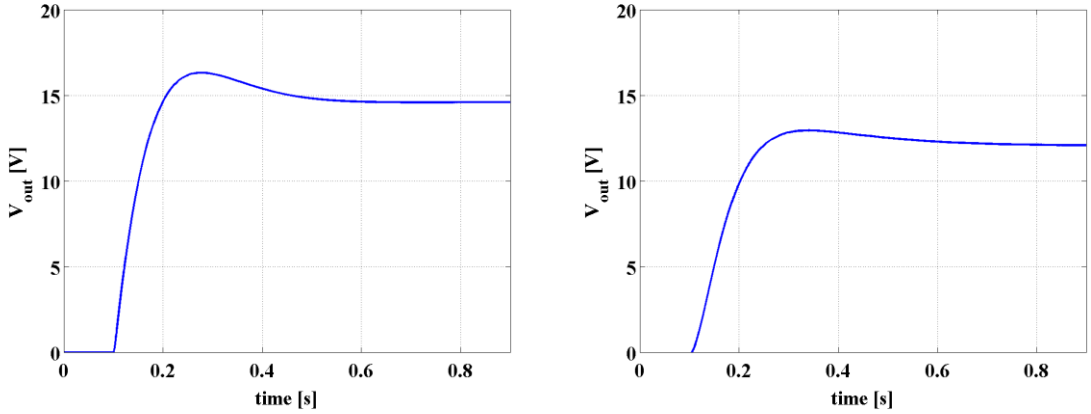

Figure 43. Trial 3 output voltage step response, experimental (left) simulation (right).

The input power of the converter was measured after the converter was turned on through the Chipscope interface, and the results are illustrated in Figure 44. An oscilloscope recorded the converter's input current and input voltage and then calculated the input power. The input power was downloaded to a PC, filtered in Matlab, and is displayed on the left. A comparable experiment was conducted on the Simulink model, and the filtered results are displayed on the right.

An underdamped response was observed in both the hardware and simulation. The experimental data revealed a slight overshoot. The simulation revealed a 4 W (26.7%) overshoot. The disparity between the overshoot is attributed to the simulation running at a higher operating point due to the losses not accounting hardware losses as discussed in Trial 1's results.

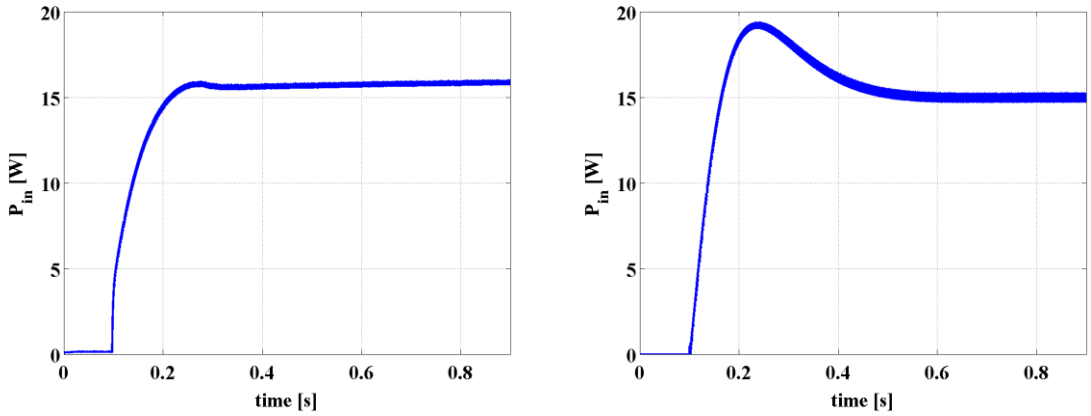

Figure 44. Trial 3 input power step response, experimental (left) simulation (right).

The steady state input power waveforms are illustrated in Figure 45. The hardware model reached steady state at 15.35 W, while the simulation achieved state at the commanded 15.01 W.

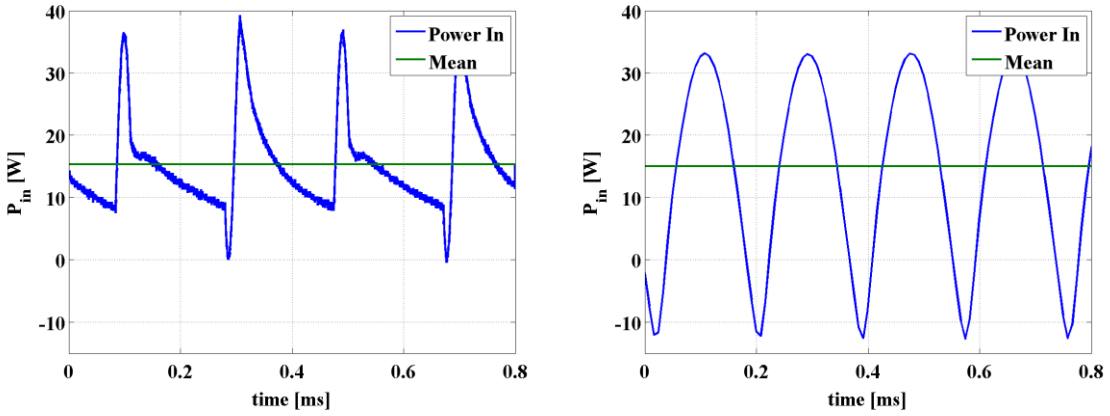

Figure 45. Trial 3 input power during steady state operation, experimental (left) and simulation (right).

The steady state output power is illustrated in Figure 46. The left plot is experimental data, and the right is from the Simulink simulation. The simulation's mean output power was 14.92 W, and the experimental output power was measured at 10.02 W. The difference between the two values is 4.90 W and is attributed to the losses realized by the IGBT and full bridge rectifier.

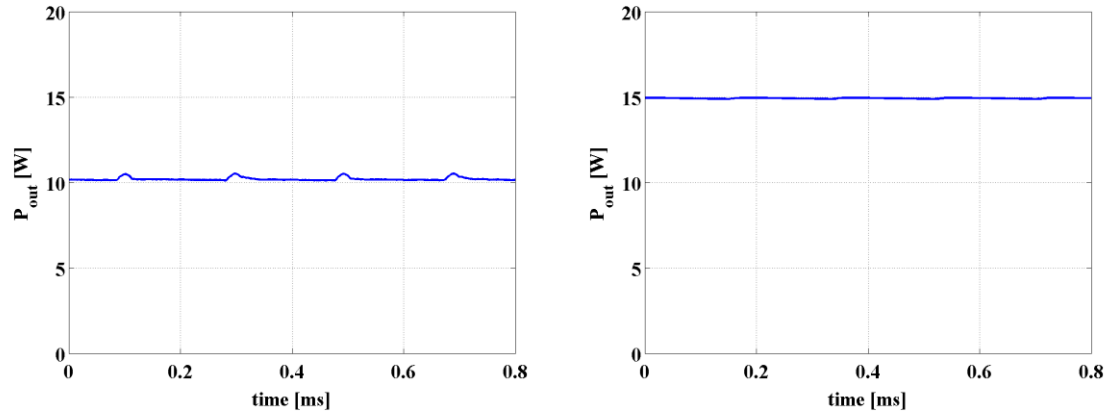

Figure 46. Trial 3 output power during steady state operation, experimental (left) and simulation (right).

The steady state resonant tank current is illustrated in Figure 47. The experimental data is displayed on the left and the simulation on the right. The experimental model operated at 2.54 kHz, while the simulation operated at 2.70 kHz. In steady state the experimental model's peak current was measured at 9.20 A, and the smaller peak was measured at 1.86 A. The simulation's peak current was measured at 9.75 A, and the smaller peak was measured at 0.80 A. The disparity between the smaller peaks is a result of the differences in output voltages between the experimental data and the simulation.

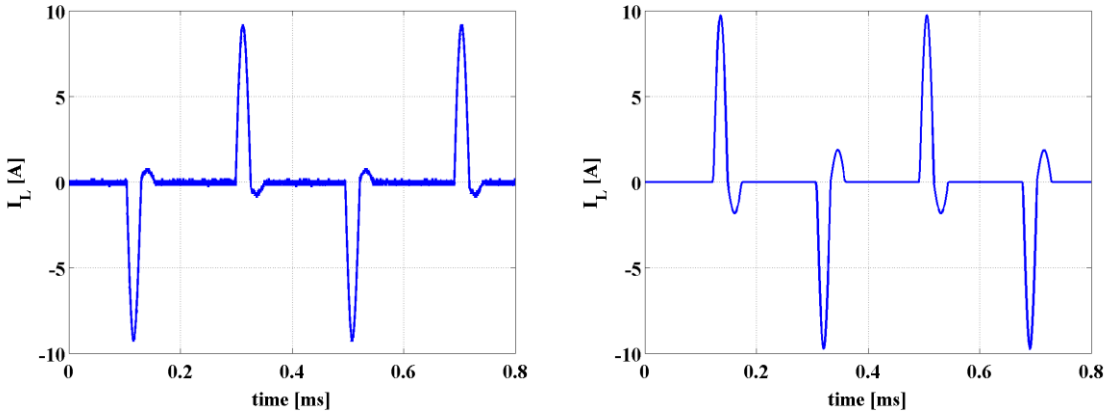

Figure 47. Trial 3 resonant tank current during steady state operation, experimental (left) and simulation (right).

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VI. CONCLUSIONS AND FUTURE RESEARCH

A. CONCLUSIONS

The days of designing systems without an accurate model are in the past. In this research a constant power SLR converter was modeled and tested in Simulink. A series of trails were conducted on the model by adjusting the PI controller's gains until desired results were achieved. With a firm understanding of the converter's performance, the Simulink code was converted into Xilinx code, downloaded to a FPGA and used to control a SLR converter.

Using a Semikron Semistack Multi-function IGBT box, the SDC in the NPS Power lab, and readily available parts, we prototyped a SLR converter. The SDC is an excellent resource for digital control of power electronics design and enables students to rapidly verify results in hardware. As a result, this research was focused on the converter being modeled, not the tools used to do the modeling.

A series of identical trails were conducted on both the Simulink model and the hardware prototype. In each case, the Simulink model accurately predicted the behavior of the converter and also proved to be very useful in tuning the converter controller. During testing disparities between the simulation and hardware output voltage and output power were identified and discussed in detail in Chapter V.

B. FUTURE RESEARCH

First, a linear state space model of the SLR converter implemented in this research would be very beneficial and provide a variety of research topics for future students.

Second, adding losses to the model and further work to enable the model to accurately predict the operation frequency of the converter are areas that would improve the model.

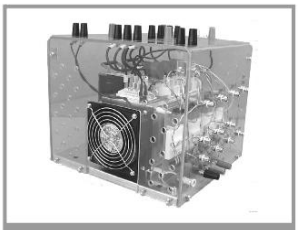
Third, implementing a more advanced control strategy that accounts for the large input power swings and allows for higher proportional gains may improve the

performance of the circuit. This may be accomplished by taking the mean value of the input power over a cycle in lieu of providing a real-time input to the PI controller.

Finally, converters used to charge a predetermined load could operate with a lookup table, which requires fewer sensors and is simpler to implement.

APPENDIX A: DATASHEETS

SEMISTACK - IGBT



SEMITRANS Stack[1)]

Three-phase rectifier + inverter with brake chopper

SEMITEACH - IGBT
SKM 50 GB 123D
SKD 51
P3/250F

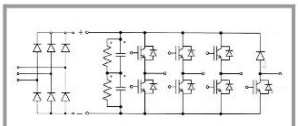
Features

- Multi-function IGBT converter
- Transparent enclosure to allow visualization of every part
- IP2x protection to minimize safety hazards
- External banana/BNC type connectors for all devices
- Integrated drive unit offering short-circuit detection/cut-off, power supply failure detection, interlock of IGBTs + galvanic isolation of the user
- Forced-air cooled heatsink

Typical Applications

- Education: One stack can simulate almost all existing industrial applications:
- 3-phase inverter+brake chopper
- Buck or boost converter
- Single phase inverter
- Single or 3-phase rectifier

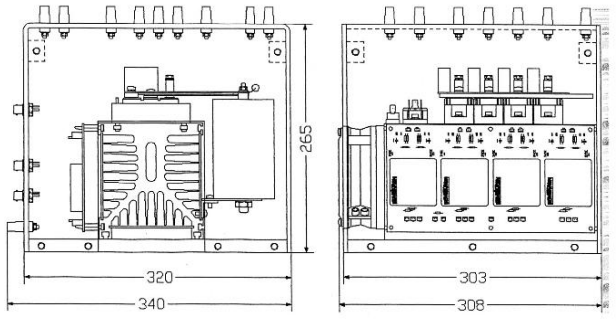
[1)] Photo non-contractual



B6U + B6CI + E1CIKF

Circuit	I_{rms} (A)	V_{ac} / V_{dcmax}	Types
B6CI	30	440 / 750	SEMITEACH - IGBT

Symbol	Conditions	Values	Units
I_{rms}	no overload	30	A
	IGBT - 4x SKM 50 GB 123D		
V_{CES}		1200	V
$V_{CE(SAT)}$	I_c= 50A, V_{GE}= 15V, chip level; T_j= 25(125)°C	2,7 (3,5)	V
V_{GES}		±20	V
I_C	T_{case}= 25 (80)°C	50 (40)	A
I_{CM}	T_{case}= 25 (80)°C; t_p= 1ms	100 (80)	A
	Rectifier - 1x SKD 51/14		
$V_{in(max)}$	without filter	3 x 480	V
	with filter	3 x 380	V
	DC Capacitor bank - Electrolytic 2x 2200µF/400V		
C_{eqvl}	total equivalent capacitance	1100 / 800	µF / V
V_{DCmax}	max. DC voltage applied to the capacitor bank	750	V
	Driver - 4x SKHI 22		
Power supply		0 / 15	V
Current consumption	max; per driver	16	mA
Thermal trip	Normally Open type (NO)	71	°C



General dimensions

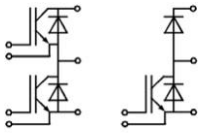
Absolute Maximum Ratings Symbol	Conditions [1]	Values ... 123 D	Units
V_{CES}		1200	V
V_{CGR}	R_{GE} = 20 kΩ	1200	V
I_C	T_{case} = 25/80 °C	50 / 40	A
I_{CM}	T_{case} = 25/80 °C; t_p = 1 ms	100 / 80	A
V_{GES}		± 20	V
P_{tot}	per IGBT, T_{case} = 25 °C	310	W
T_j, (T_{stg})		– 40 . . .+150 (125)	°C
V_{isol}	AC, 1 min.	2 500	V
humidity	DIN 40 040	Class F	
climate	DIN IEC 68 T.1	40/125/56	
Diodes			
I_F= – I_C	T_{case} = 25/80 °C	50 / 40	A
I_{FM}= – I_{CM}	T_{case} = 25/80 °C; t_p = 1 ms	100 / 80	A
I_{FSM}	t_p = 10 ms; sin.; T_j = 150 °C	550	
I^2t	t_p = 10 ms; T_j = 150 °C	1500	A^2s

Characteristics Symbol	Conditions [1]	min.	typ.	max.	Units
$V_{(BR)CES}$	V_{GE} = 0, I_C = 1 mA	≥ V_{CES}	–	–	V
$V_{GE(th)}$	V_{GE} = V_{CE}, I_C = 2 mA	4,5	5,5	6,5	V
I_{CES}	V_{GE} = 0, T_j = 25 °C	–	0,3	1	mA
	V_{CE} = V_{CES}, T_j = 125 °C	–	3	–	mA
I_{GES}	V_{GE} = 20 V, V_{CE} = 0	–	–	200	nA
V_{CEsat}	I_C = 40 A; V_{GE} = 15 V; T_j = 25 (125) °C	–	2,5(3,1)	3(3,7)	V
V_{CEsat}	I_C = 50 A; V_{GE} = 15 V; T_j = 25 (125) °C	–	2,7(3,5)	–	V
g_{fs}	V_{CE} = 20 V, I_C = 40 A		30	–	S
C_{CHC}	per IGBT	–	–	350	pF
C_{ies}	V_{GE} = 0	–	3300	4000	pF
C_{oes}	V_{CE} = 25 V	–	500	600	pF
C_{res}	f = 1 MHz	–	220	300	pF
L_{CE}		–	–	30	nH
$t_{d(on)}$	V_{CC} = 600 V	–	70	–	ns
t_r	V_{GE} = + 15 V / - 15 V [3]	–	60	–	ns
$t_{d(off)}$	I_C = 40 A, ind. load	–	400	–	ns
t_f	R_{Gon} = R_{Goff} = 27 Ω	–	45	–	ns
E_{on} [5]	T_j = 125 °C	–	7	–	mWs
E_{off} [5]		–	4,5	–	mWs
Diodes [8]					
V_F = V_{EC}	I_F = 40 A; V_{GE} = 0 V; T_j = 25 (125) °C	–	1,85(1,6)	2,2	V
V_F = V_{EC}	I_F = 50 A; V_{GE} = 0 V; T_j = 25 (125) °C	–	2,0(1,8)	–	V
V_{TO}	T_j = 125 °C	–	–	1,2	V
r_T	T_j = 125 °C	–	–	22	mΩ
I_{RRM}	I_F = 40 A; Tj = 25 (125) °C [2]	–	23(35)	–	A
Q_{rr}	I_F = 40 A; T_j = 25 (125) °C [2]	–	2,3(7)	–	µC
Thermal Characteristics					
R_{thjc}	per IGBT	–	–	0,4	°C/W
R_{thjc}	per diode	–	–	0,7	°C/W
R_{thch}	per module	–	–	0,05	°C/W

SEMITRANS® M IGBT Modules

SKM 50 GB 123 D
SKM 50 GAL 123 D

SEMITRANS 2



GB GAL

Features

- MOS input (voltage controlled)
- N channel, Homogeneous Si
- Low inductance case
- Very low tail current with low temperature dependence
- High short circuit capability, self limiting to 6 * I_{cnom}
- Latch-up free
- Fast & soft inverse CAL diodes [8]
- Isolated copper baseplate using DCB Direct Copper Bonding Technology
- Large clearance (10 mm) and creepage distances (20 mm).

Typical Applications: → **B 6 - 85**

- Three phase inverter drives
- Switching (not for linear use)

1) T_{case} = 25 °C, unless otherwise specified
2) I_F = – I_C, V_R = 600 V, – di_F/dt = 800 A/µs, V_{GE} = 0 V
3) Use V_{GEoff} = -5 ... -15 V
5) See fig. 2 + 3; R_{Goff} = 27 Ω
8) CAL = Controlled Axial Lifetime Technology.

Case and mech. data → **B 6 - 86**
SEMITRANS 2

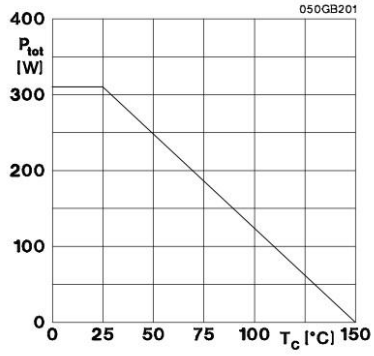
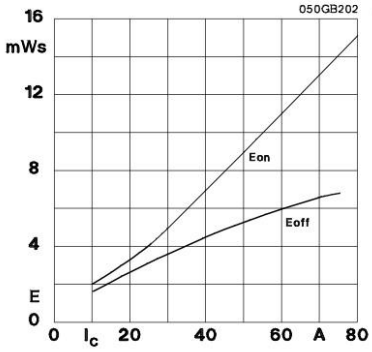
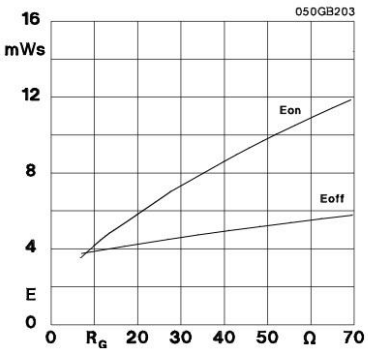


Fig. 1 Rated power dissipation $P_{tot} = f(T_C)$



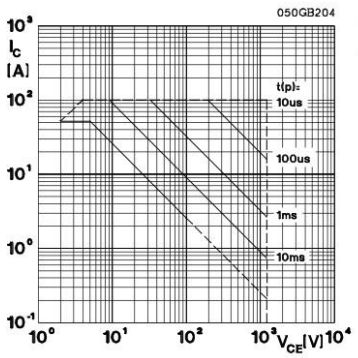
T_j = 125 °C
V_{CE} = 600 V
V_{GE} = ± 15 V
R_G = 27 Ω

Fig. 2 Turn-on /-off energy = f (I_C)



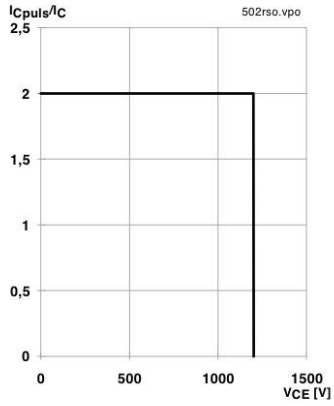
T_j = 125 °C
V_{CE} = 600 V
V_{GE} = ± 15 V
I_C = 40 A

Fig. 3 Turn-on /-off energy = f (R_G)



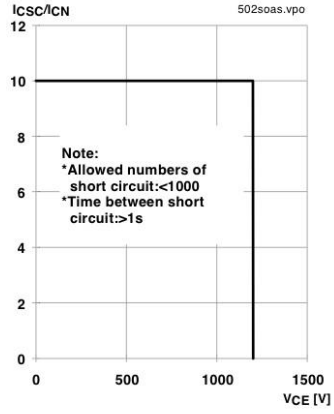
1 pulse
T_C = 25 °C
$T_j \leq$ 150 °C

Fig. 4 Maximum safe operating area (SOA) $I_C = f(V_{CE})$



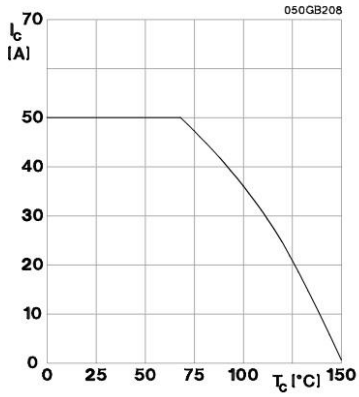
$T_j \leq$ 150 °C
V_{GE} = ± 15 V
R_{Goff} = 27 Ω
I_C = 40 A

Fig. 5 Turn-off safe operating area (RBSOA)



$T_j \leq$ 150 °C
V_{GE} = ± 15 V
$t_{sc} \leq$ 10 µs
L < 25 nH
I_{CN} = 40 A

Fig. 6 Safe operating area at short circuit $I_C = f(V_{CE})$



T_j = 150 °C
$V_{GE} \geq$ 15 V

Fig. 8 Rated current vs. temperature $I_C = f(T_C)$

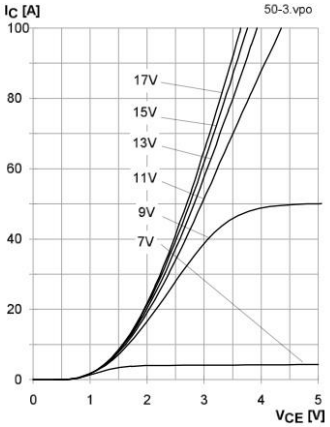


Fig. 9 Typ. output characteristic, t_p = 80 µs; 25 °C

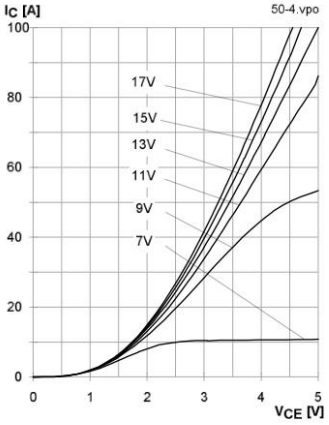


Fig. 10 Typ. output characteristic, t_p = 80 µs; 125 °C

$P_{cond(t)} = V_{CEsat(t)} \cdot I_{C(t)}$

$V_{CEsat(t)} = V_{CE(TO)(Tj)} + r_{CE(Tj)} \cdot I_{C(t)}$

$V_{CE(TO)(Tj)} \leq 1{,}5 + 0{,}002\ (T_j - 25)$ [V]

typ.: $r_{CE(Tj)} = 0{,}02 + 0{,}00008\ (T_j - 25)$ [Ω]

max.: $r_{CE(Tj)} = 0{,}03 + 0{,}00010\ (T_j - 25)$ [Ω]

valid for $V_{GE} = +15\ ^{+2}_{-1}$ [V]; $I_C > 0{,}3\ I_{Cnom}$

Fig. 11 Saturation characteristic (IGBT)
Calculation elements and equations

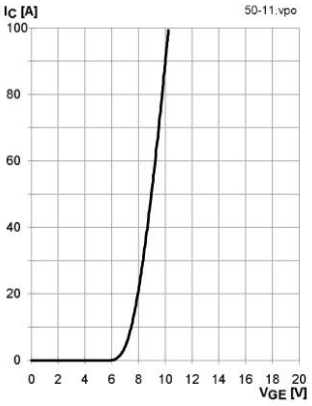


Fig. 12 Typ. transfer characteristic, t_p = 80 µs; V_{CE} = 20 V

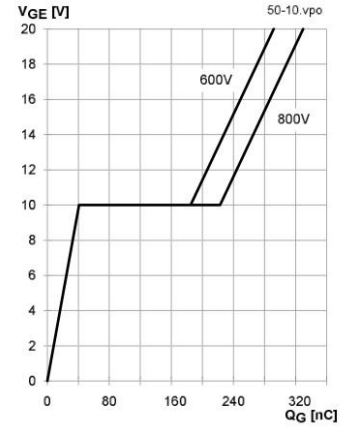
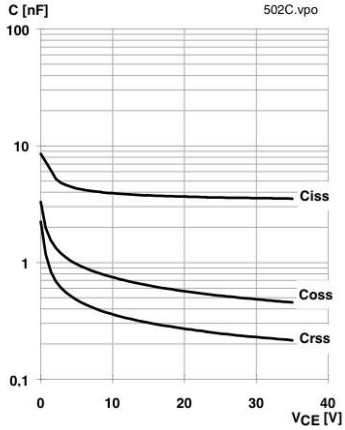


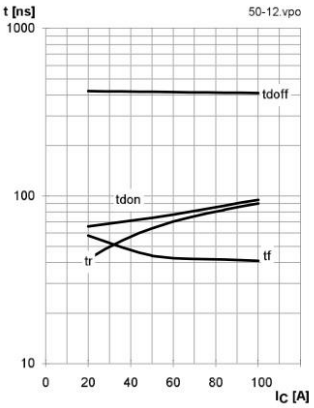
Fig. 13 Typ. gate charge characteristic

I_{Cpuls} = 50 A



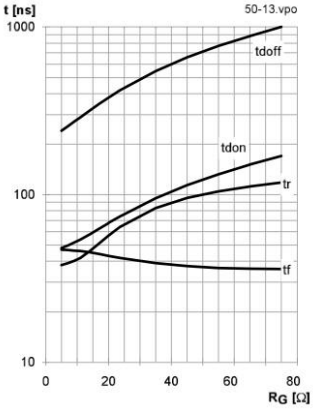
V_{GE} = 0 V
f = 1 MHZ

Fig. 14 Typ. capacitances vs.V_{CE}



T_j = 125 °C
V_{CE} = 600 V
V_{GE} = ± 15 V
R_{Gon} = 27 Ω
R_{Goff} = 27 Ω
induct. load

Fig. 15 Typ. switching times vs. I_C



T_j = 125 °C
V_{CE} = 600 V
V_{GE} = ± 15 V
I_C = 40 A
induct. load

Fig. 16 Typ. switching times vs. gate resistor R_G

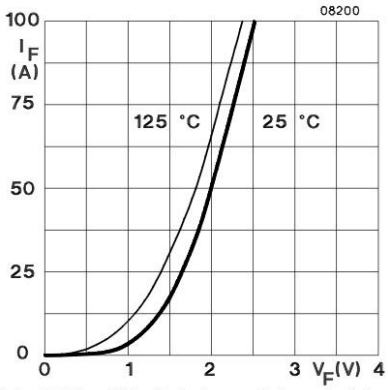


Fig. 17 Typ. CAL diode forward characteristic

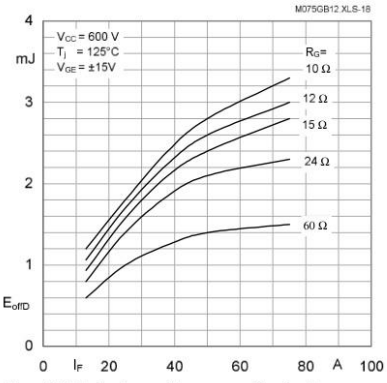


Fig. 18 Diode turn-off energy dissipation per pulse

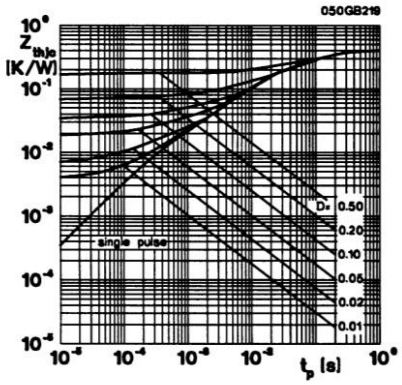


Fig. 19 Transient thermal impedance of IGBT
$Z_{thJC} = f(t_p)$; $D = t_p / t_c = t_p \cdot f$

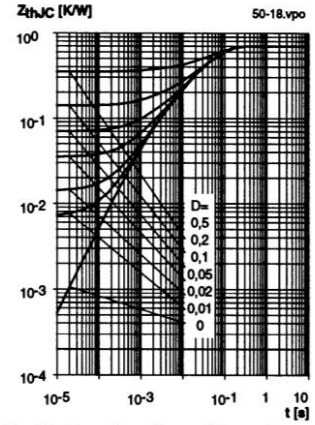


Fig. 20 Transient thermal impedance of inverse CAL diodes $Z_{thJC} = f(t_p)$; $D = t_p / t_c = t_p \cdot f$

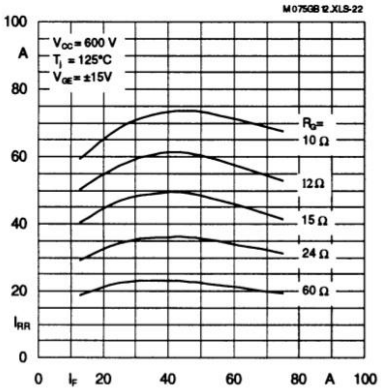


Fig. 22 Typ. CAL diode peak reverse recovery current
$I_{RR} = f(I_F, R_G)$

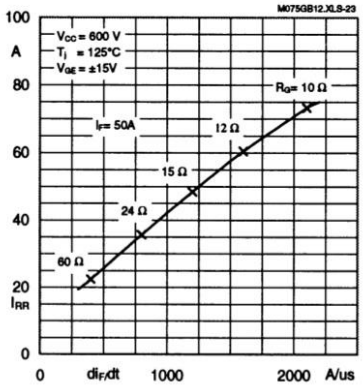


Fig. 23 Typ CAL diode peak reverse recovery current
$I_{RR} = f(di/dt)$

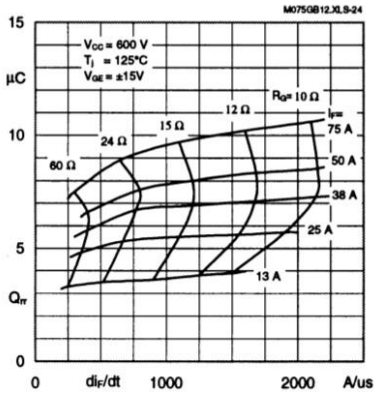


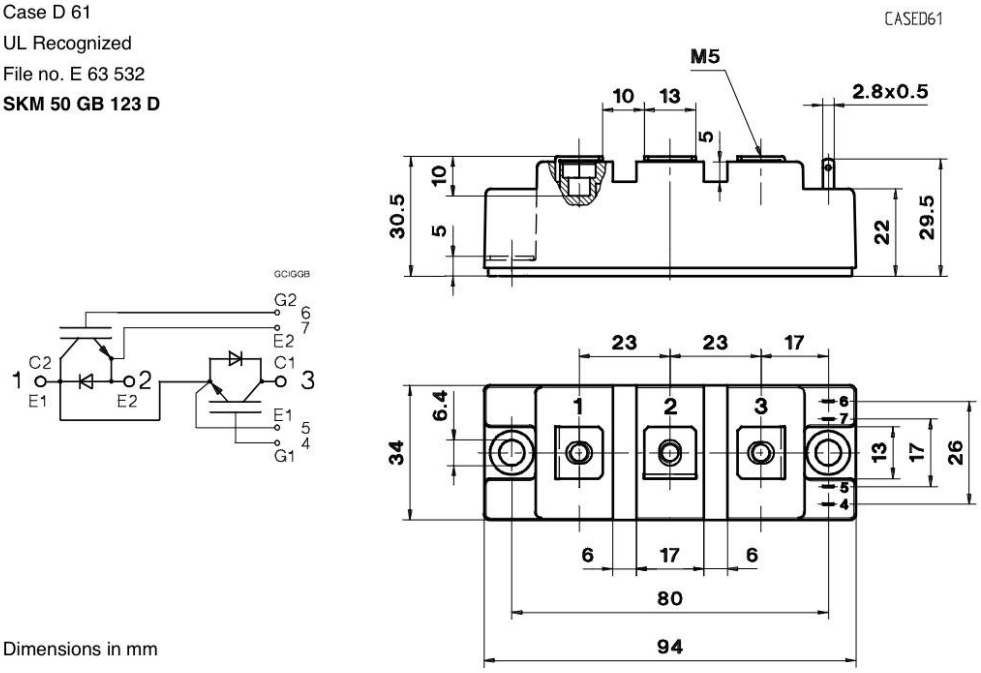
Fig. 24 Typ. CAL diode recovery charge

Typical Applications

include

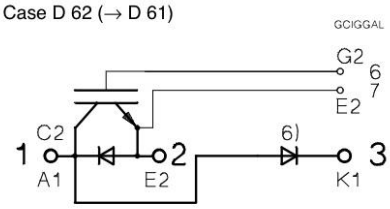
Switched mode power supplies
DC servo and robot drives
Inverters
DC choppers
AC motor speed control
Inductive heating
UPS Uninterruptable power supplies
General power switching applications
Electronic (also portable) welders
Pulse frequencies also above 15 kHz

SEMITRANS 2
Case D 61
UL Recognized
File no. E 63 532
SKM 50 GB 123 D



Dimensions in mm

SKM 50 GAL 123 D
Case D 62 (→ D 61)



Case outline and circuit diagrams

Mechanical Data						
Symbol	Conditions		Values			Units
			min.	typ.	max.	
M_1	to heatsink, SI Units	(M6)	3	–	5	Nm
	to heatsink, US Units		27	–	44	lb.in.
M_2	for terminals, SI Units	(M5)	2,5	–	5	Nm
	for terminals US Units		22	–	44	lb.in.
a			–	–	5x9,81	m/s^2
w			–	–	160	g

This is an electrostatic discharge sensitive device (ESDS). Please observe the international standard IEC 747-1, Chapter IX.

Eight devices are supplied in one SEMIBOX A without mounting hardware, which can be ordered separately under Ident No. 33321100 (for 10 SEMITRANS 2)
Larger packaging units of 20 or 42 pieces are used if suitable
Accessories → B 6 – 4.
SEMIBOX → C – 1.

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APPENDIX B: MATLAB M-FILES

A. MATLAB INITIAL CONDITIONS FILE

SLR_IC.m

```
open_loop=0 ;

Ki=900;
Kp=5;
f_ref_ic=3000;
P_ref=15;
Lin=20e-6;
Lres=30e-6;
Cres=2.2e-6;

Cout=2*2000e-6;
R_load=1/(1/50+1/20+1/20);
%R_load=1/(1/50+1/20)

Vdc=43;
Vcout_ic=0;
Ki_ic=0;

step_ct=1;
f_clock=60e6;
tstep = step_ct/f_clock;
wdt=90420/f_clock*step_ct;
dt=1/f_clock*step_ct;
fin=100;

wo=1/sqrt(Lres*Cres)
fo=wo/(2*pi)
fohalf=fo*.5
Zo=sqrt(Lres/Cres)
tstep = step_ct/f_clock;
F_mat = [0 0 0 1;1 1 2 0;2 2 3 0;3 3 0 0];
O_mat = F_mat;
```

B. RUNNING A SIMULINK MODEL FROM THE WORKSPACE

LOOP_PI.M

```
%Use this file to run a Simulink model from the command
%line.  For multiple jobs, put this code into a loop and
%save the output of each trial.  Ensure that you comment
%out the values that will be put into the loop in the
%initial conditions file, otherwise they will overwrite the
%values being changed in the loop.

mdl='EC4150_lab3_SLR_RBL3';
load_system(mdl)
set_param(mdl,'SimulationMode','Accelerator')
warning('off','Simulink:SL_UINotUpdatedDuringRapidAccelSim'
)
R_load=1/(1/50+1/20+1/20)
Kp=5;
Ki=600;
Vdc=43;
Cout=4000e-6;
sim(mdl,[0 1.5])
```

C. CHIPSCOPE TO MATLAB INTERFACE

dataplot_loadres_rbl.m

```
%Alex Julian
%This file takes the output of chipscope and formats it for
%matlab.  The scaling factors are in place to reverse any
%scaling that was required by the Simulink chipscope
%interface.

datain=importdata('data.prn');
vecsize=length(datain.data);
deltat=180/25e6;
datasize=vecsize-1;
adc1raw=zeros(1,datasize);%Channel 1
adc2raw=zeros(1,datasize);%Channel 2
adc3raw=zeros(1,datasize);%Channel 3
adc4raw=zeros(1,datasize);%Channel 4

for ii=1:datasize
    index=ii+vecsize-datasize-1;

adc1raw(ii)=datain.data(index,1+2)+2*datain.data(index,2+2)
+2^2*datain.data(index,3+2)+2^3*datain.data(index,4+2)+2^4*
datain.data(index,5+2)+2^5*datain.data(index,6+2)+2^6*datai
n.data(index,7+2)+2^7*datain.data(index,8+2)+2^8*datain.dat
a(index,9+2)+2^9*datain.data(index,10+2)+2^10*datain.data(i
ndex,11+2)+2^11*datain.data(index,12+2);

adc2raw(ii)=datain.data(index,1+14)+2*datain.data(index,2+1
4)+2^2*datain.data(index,3+14)+2^3*datain.data(index,4+14)+
2^4*datain.data(index,5+14)+2^5*datain.data(index,6+14)+2^6
*datain.data(index,7+14)+2^7*datain.data(index,8+14)+2^8*da
tain.data(index,9+14)+2^9*datain.data(index,10+14)+2^10*dat
ain.data(index,11+14)+2^11*datain.data(index,12+14);

adc3raw(ii)=datain.data(index,1+26)+2*datain.data(index,2+2
6)+2^2*datain.data(index,3+26)+2^3*datain.data(index,4+26)+
2^4*datain.data(index,5+26)+2^5*datain.data(index,6+26)+2^6
*datain.data(index,7+26)+2^7*datain.data(index,8+26)+2^8*da
tain.data(index,9+26)+2^9*datain.data(index,10+26)+2^10*dat
ain.data(index,11+26)+2^11*datain.data(index,12+26);
```

```
adc4raw(ii)=datain.data(index,1+38)+2*datain.data(index,2+3
8)+2^2*datain.data(index,3+38)+2^3*datain.data(index,4+38)+
2^4*datain.data(index,5+38)+2^5*datain.data(index,6+38)+2^6
*datain.data(index,7+38)+2^7*datain.data(index,8+38)+2^8*da
tain.data(index,9+38)+2^9*datain.data(index,10+38)+2^10*dat
ain.data(index,11+38)+2^11*datain.data(index,12+38);
end

%Data scaled according to the Simulink Chipscope interface
%block.

adc1=(adc1raw/2^3-100);
adc2=(adc2raw/2^-1);
adc3=(adc3raw/2^3-100);
adc4=(adc4raw/2^6-10);

time=[0:datasize-1]*deltat;

figure;
plot(time,adc1);
mean(adc1)

figure;
plot(time,adc2);
mean(adc2)

figure;
plot(time,adc3);
mean(adc3)

figure;
plot(time,adc4);
mean(adc4)
```

D. OSCILLOSCOPE TO MATLAB INTERFACE

importfile.m

```
%This function formats the csv file from the scope for
%matlab.

function importfile(fileToRead1)
%IMPORTFILE(FILETOREAD1)
%  Imports data from the specified file
%  FILETOREAD1:  file to read
%  Auto-generated by MATLAB on 01-Apr-2011 11:36:59
DELIMITER = ',';
HEADERLINES = 15;
% Import the file
newData1 = importdata(fileToRead1, DELIMITER, HEADERLINES);
% Create new variables in the base workspace from those
fields.
vars = fieldnames(newData1);
for i = 1:length(vars)
    assignin('base', vars{i}, newData1.(vars{i}));
end
```

scope_formatting.m

```
%this file calls the importfile function and creates the
%variables used to create the plots in this research.

fileToRead1='Tek_CH1_Wfm.csv'
importfile(fileToRead1)
Voltage=data(:,2)';
Voltage=Voltage(:,1:length(Voltage)-1);
fileToRead1='Tek_CH2_Wfm.csv'
importfile(fileToRead1)
Current=data(:,2)';
Current=Current(:,1:length(Current)-1);

fileToRead1='Tek_CH3_Wfm.csv'
importfile(fileToRead1)
Vout=data(:,2)';
Vout=Vout(:,1:length(Vout)-1);

fileToRead1='Tek_MATH_Wfm.csv'
importfile(fileToRead1)
Power=data(:,2)';
```

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